

2013 S-Series Intel Shark Bay

UMA/DIS Muxless Schematic
14.0''Rampage 15.6''Renegade 17.0''Ricochet

Haswell-M Dual/Quad Core SV
rPGA947 37W
Lynx Point-M PCH

REV:MV
2013-08-01

DY:No stuff
DIS_PX:Only DIS install

WWW.MANUALS.CLAN.SU

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Cover Page

Size
A4

Document Number

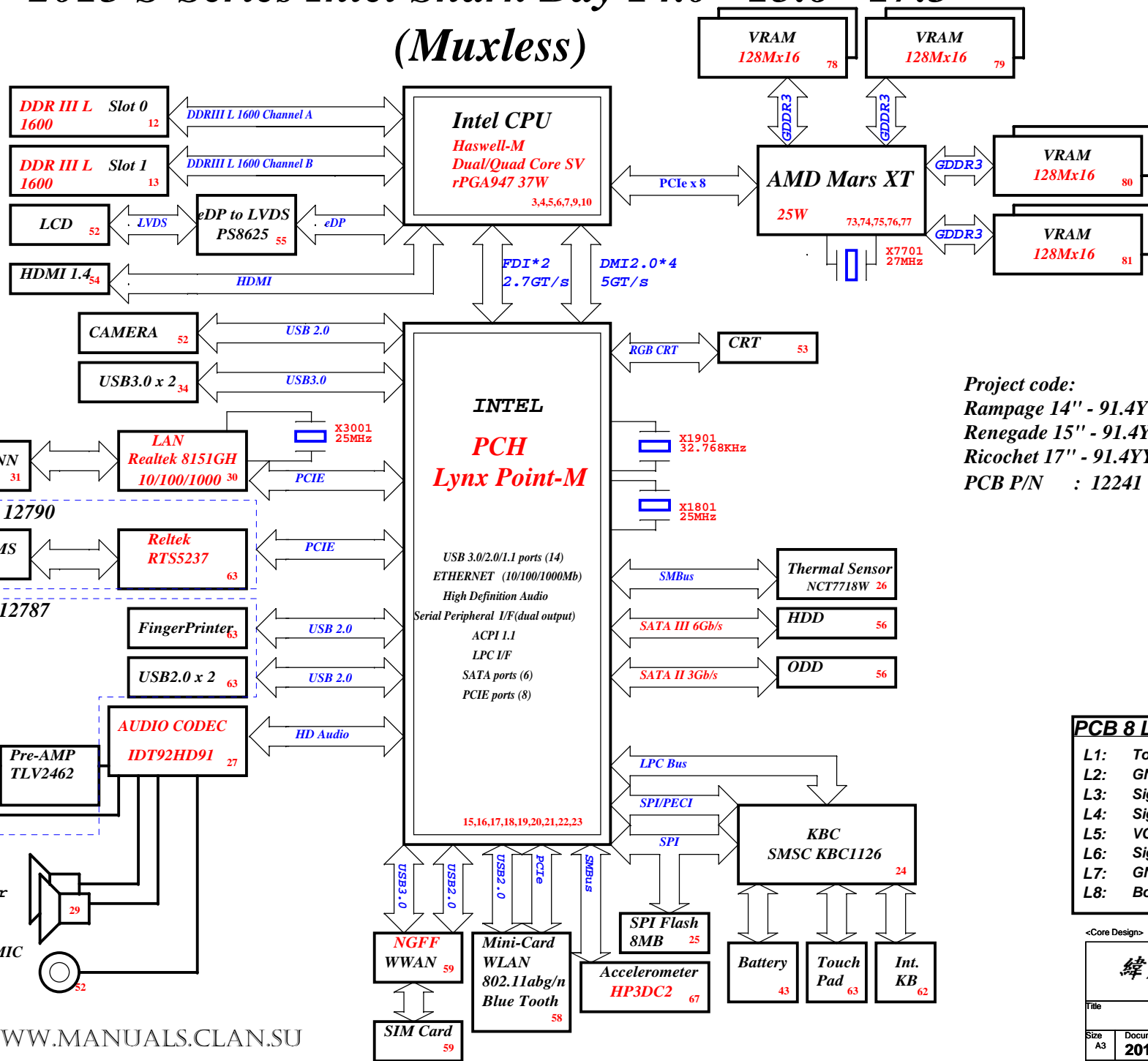
2013 S-Series Shark Bay 14 15 17

Rev
1

Date: Thursday, August 01, 2013

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2013 S-Series Intel Shark Bay 14.0" 15.6" 17.3"
(Muxless)



Project code:
Rampage 14" - 91.4YW01.001
Renegade 15" - 91.4YX01.001
Ricochet 17" - 91.4YY01.001
PCB P/N : 12241

| | |
|-----------------------------|--|
| CPU DC/DC | |
| TPS51631RSMR 46,47 | |
| INPUTS | OUTPUTS |
| DCBATOUT | VCC_CORE |
| SYSTEM DC/DC | |
| TPS51367RVER 48 | |
| INPUTS | OUTPUTS |
| DCBATOUT | 1D05V_VIT |
| SYSTEM DC/DC | |
| RT8223MZQW 45 | |
| INPUTS | OUTPUTS |
| DCBATOUT | 5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 |
| SYSTEM DC/DC | |
| TPS51216RUKR 49 | |
| INPUTS | OUTPUTS |
| DCBATOUT | 1D35V_S3 0D675V_S0 DDR_VREF_S3 |
| SYSTEM DC/DC | |
| APL5930KAI 51 | |
| INPUTS | OUTPUTS |
| 3D3V_S5 | 1D5V_S0 |
| VGA | |
| ADP3211MNR2G 82 | |
| INPUTS | OUTPUTS |
| DCBATOUT | VGA_CORE |
| CHARGER | |
| BQ24736RGRR 44 | |
| INPUTS | OUTPUTS |
| AD+ BT+ | DCBATOUT |
| VGA | |
| G9661-25ADJF11U 83 | |
| INPUTS | OUTPUTS |
| 3D3V_S0 | 1D8V_VGA_S0 |
| VGA | |
| APL5930KAI 83 | |
| INPUTS | OUTPUTS |
| 1D35V_S3 | 0D95V_VGA_S0 |
| Switches 36,83 | |
| INPUTS | OUTPUTS |
| 5V_S5 3D3V_S5 3D3V_S0 | 5V_S0 3D3V_S0 3D3V_VGA |
| VGA | |
| TPS51211DSCR | |
| INPUTS | OUTPUTS |
| DCBATOUT | 1D5V_VGA_S0 |

PCB 8 LAYER

- L1:** *Top*
L2: *GND*
L3: *Signal*
L4: *Signal*
L5: *VCC*
L6: *Signal*
L7: *GND*
L8: *Bottom*

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Title

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Block Diagram

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2013 S-Series Shark Bay 14 15 17

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SSID = CPU

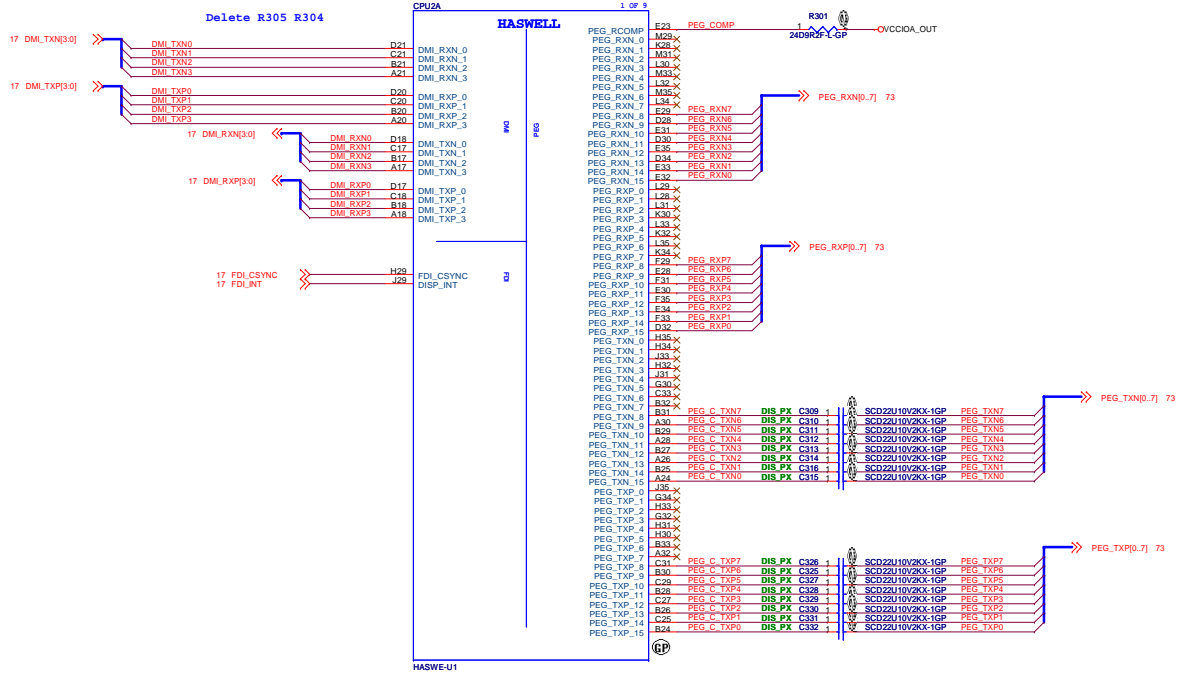
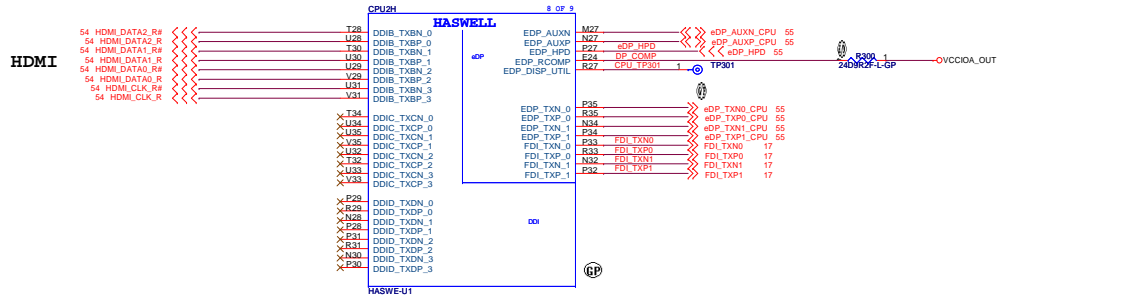
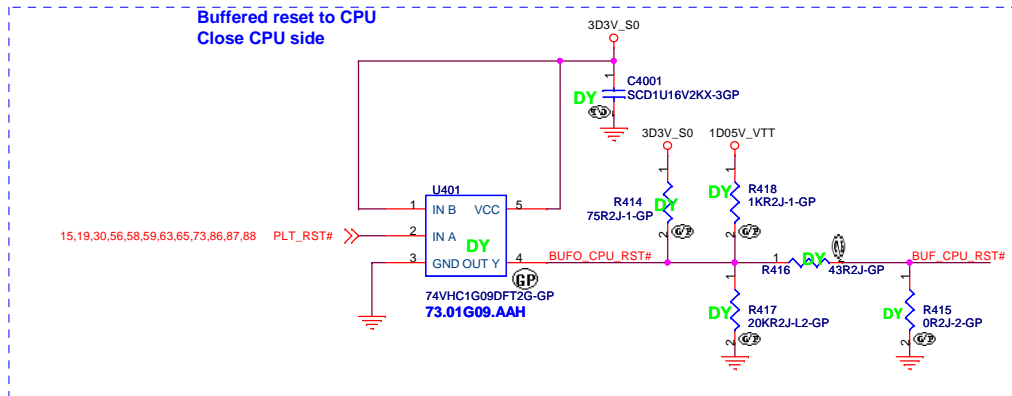
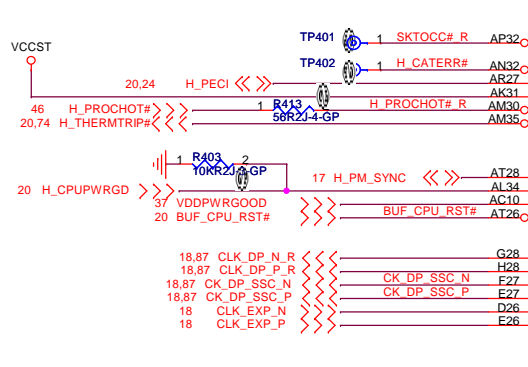
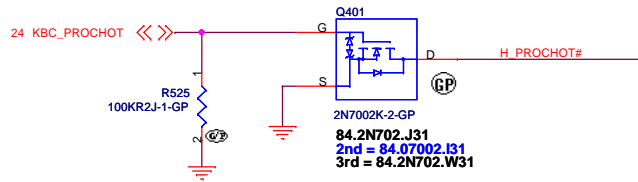
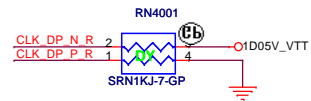
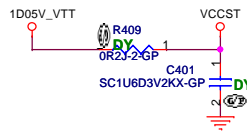
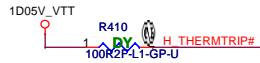
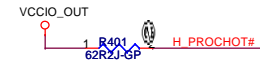


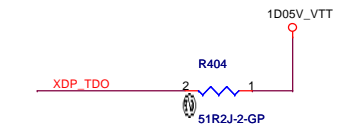
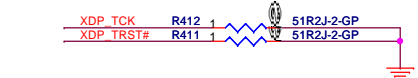
Table showing Physical Link Width, Negotiated Link Width, Physical SMI Lanes, and Processor. The table includes columns for Physical Link Width, Negotiated Link Width, Physical SMI Lanes, and Processor. The table is used to determine the link width for various processors.



SSID = CPU



Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

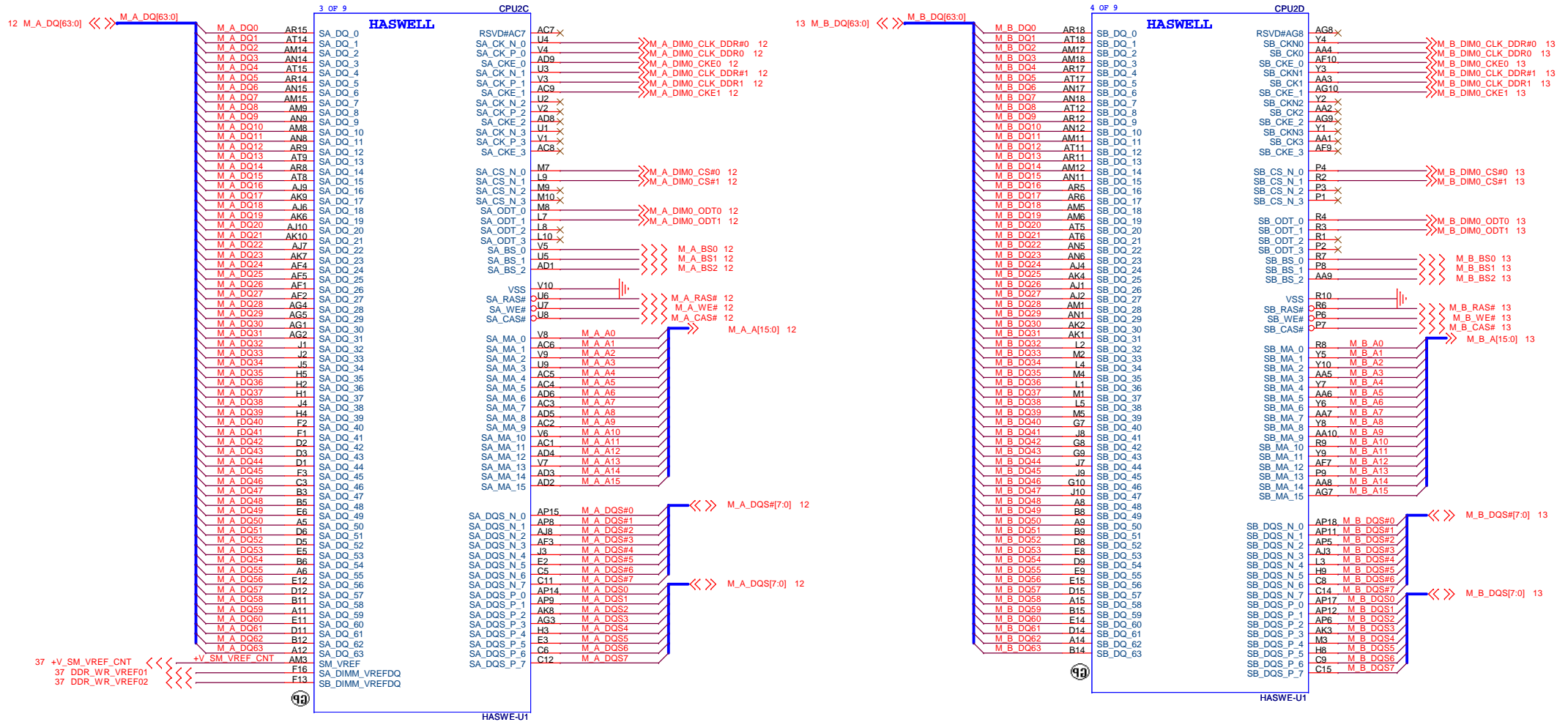


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| CPU (THERMAL/CLOCK/PM) | | | |
|------------------------|----------------------------------|-------|----------|
| Size | Document Number | Rev | |
| A3 | 2013 S-Series Shark Bay 14 15 17 | 1 | |
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SSID = CPU



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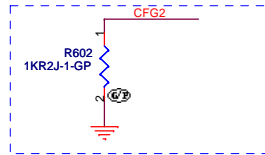
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| | | | |
|------------------|---|----------|----------|
| Title | | | |
| CPU (DDR) | | | |
| Size A3 | Document Number | Rev | |
| | 2013 S-Series Shark Bay 14 15 17 | 1 | |
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SSID = CPU

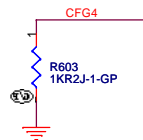
PEG Static Lane Reversal

CFG2 1: Normal Operation; Lane # definition matches socket pin map definition
0: Lane Reversed



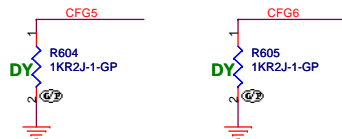
eDP Enable

CFG4 1: Disable
0: Enable



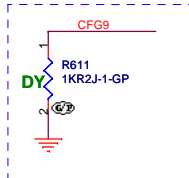
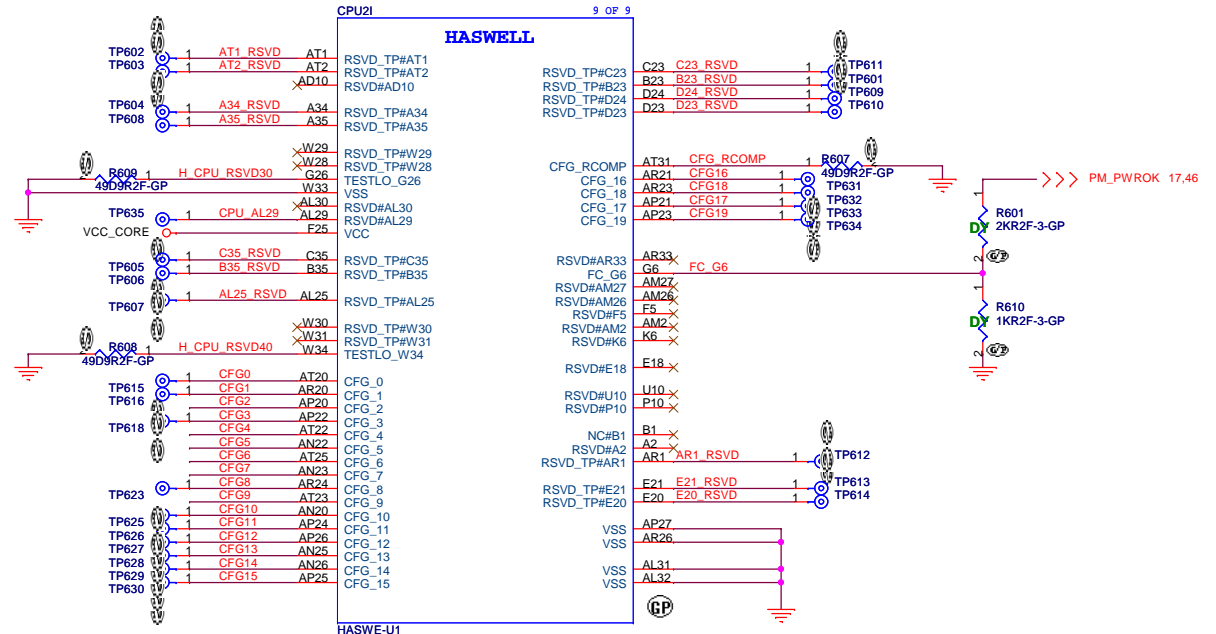
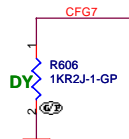
PCIe Port Bifurcation Straps

CFG[6:5] 11: x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING

CFG7 1: PEG Train immediately following xxRESETB de assertion
0: PEG Wait for BIOS for training

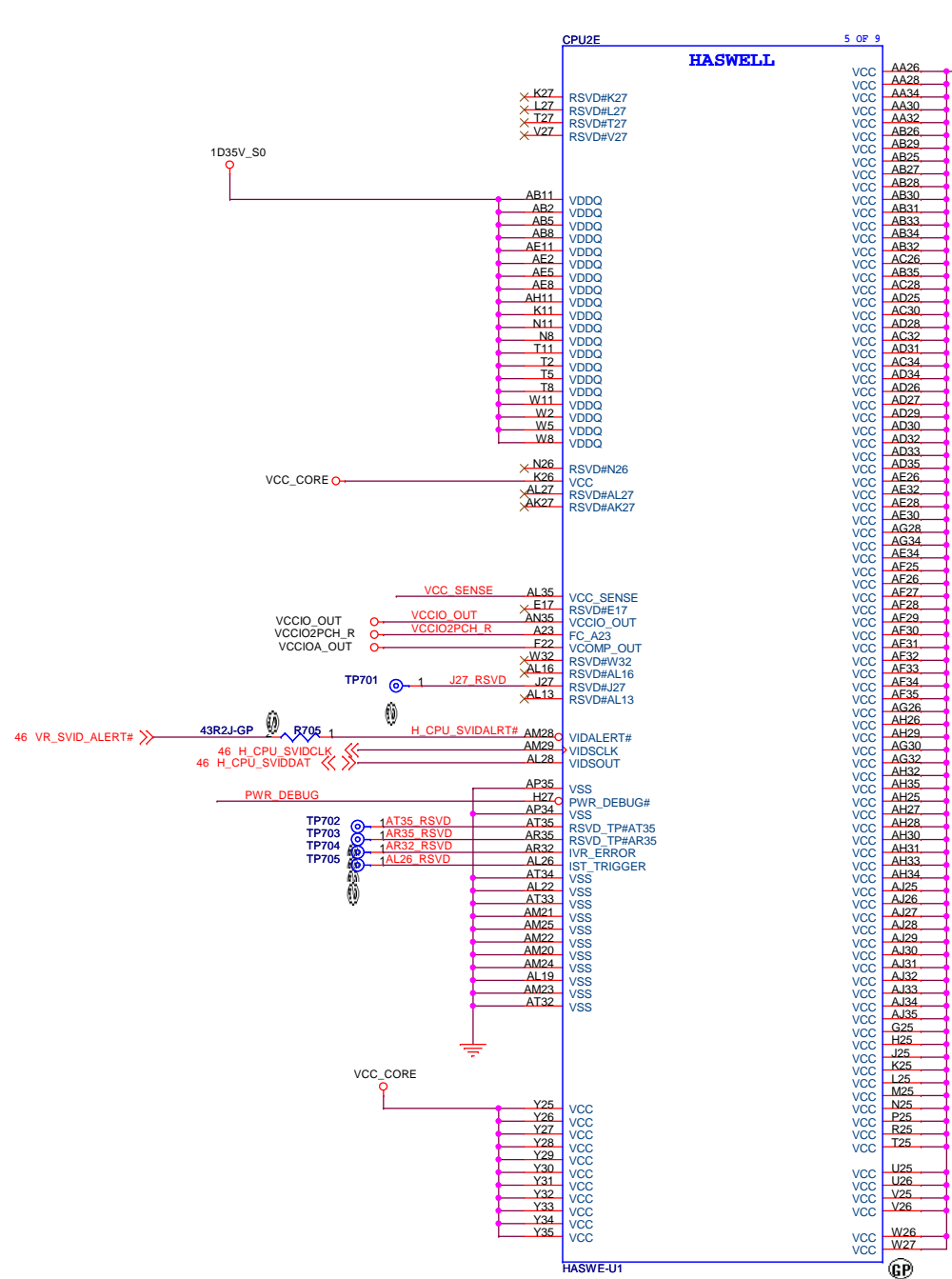
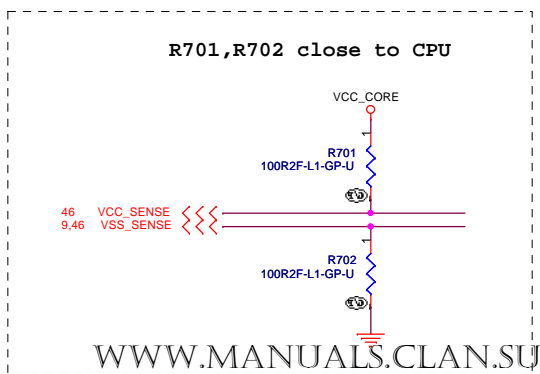
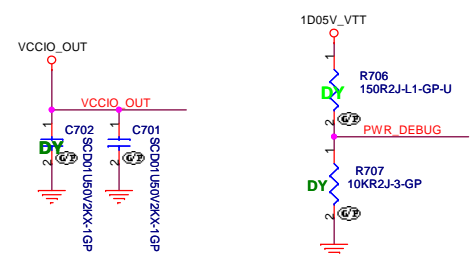
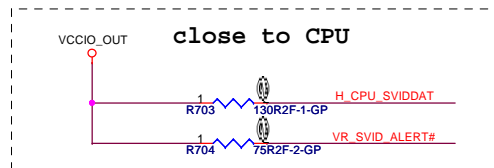
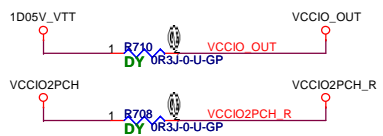


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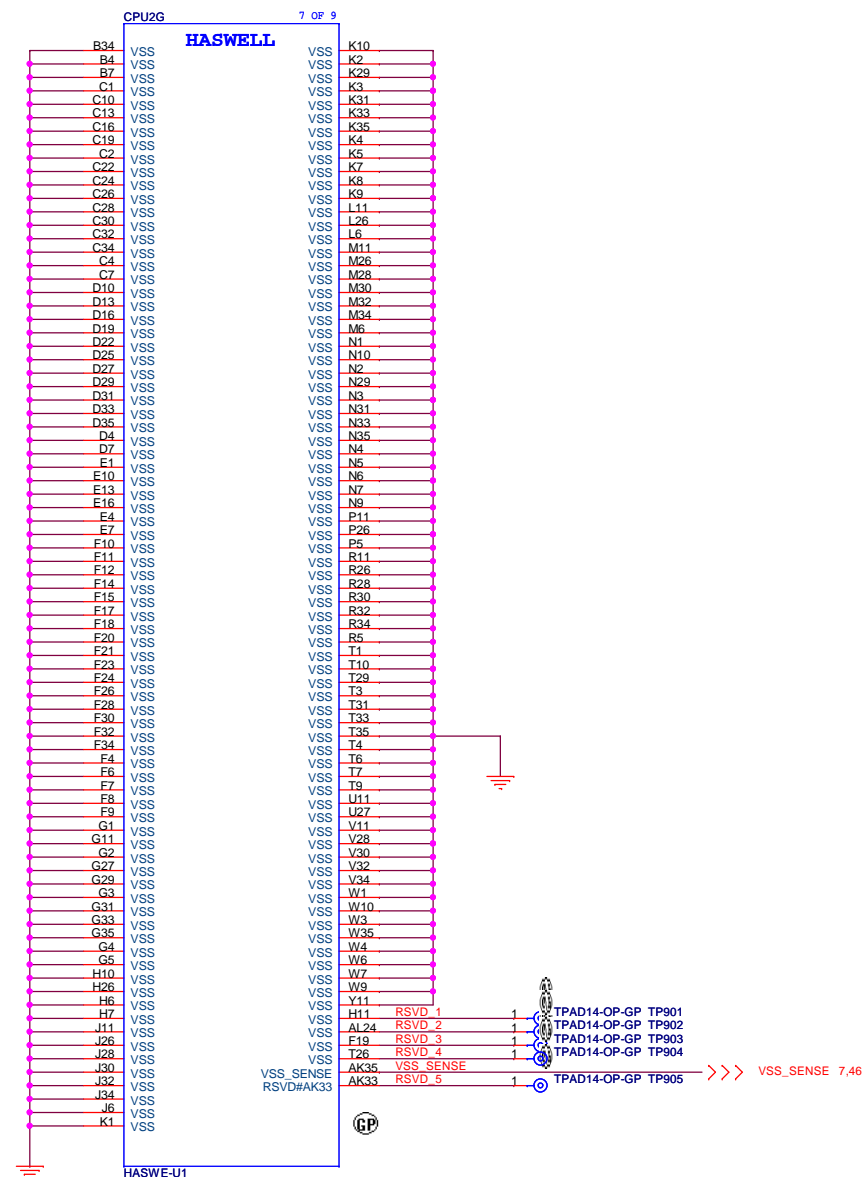
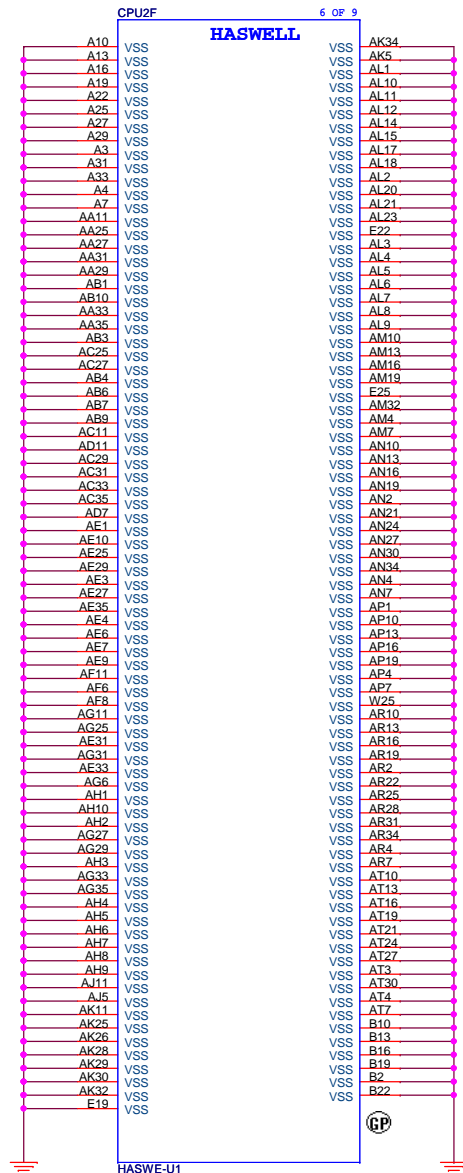
| Title | | | |
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| CPU (RESERVED) | | | |
| Size | Document Number | Rev | |
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SSID = CPU



(Reserved)

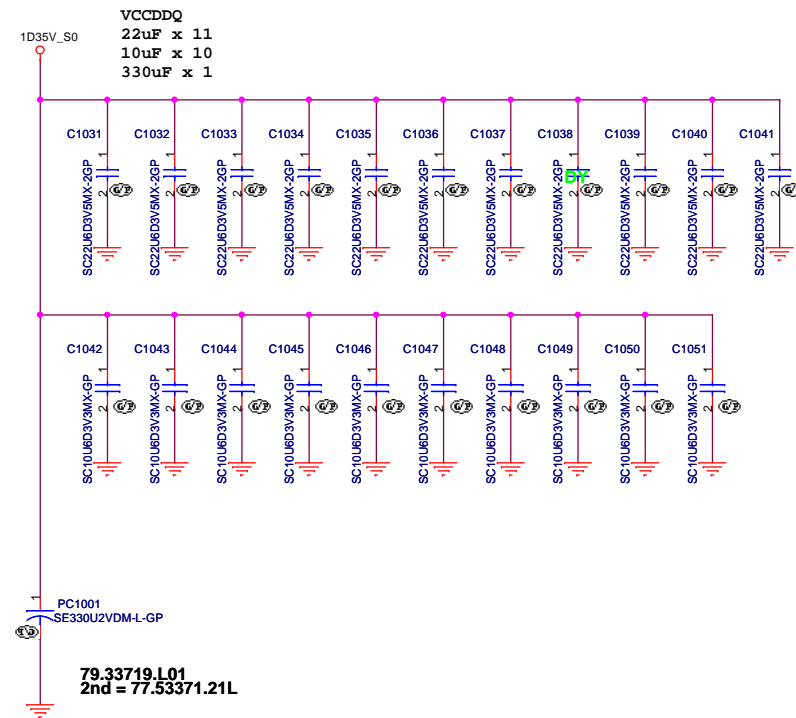
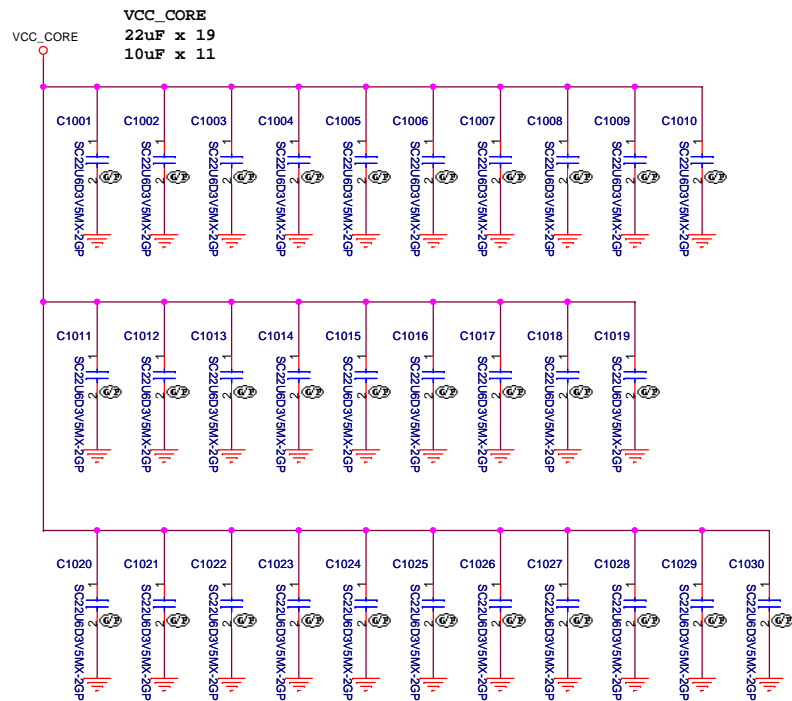
SSID = CPU



<Core Design>

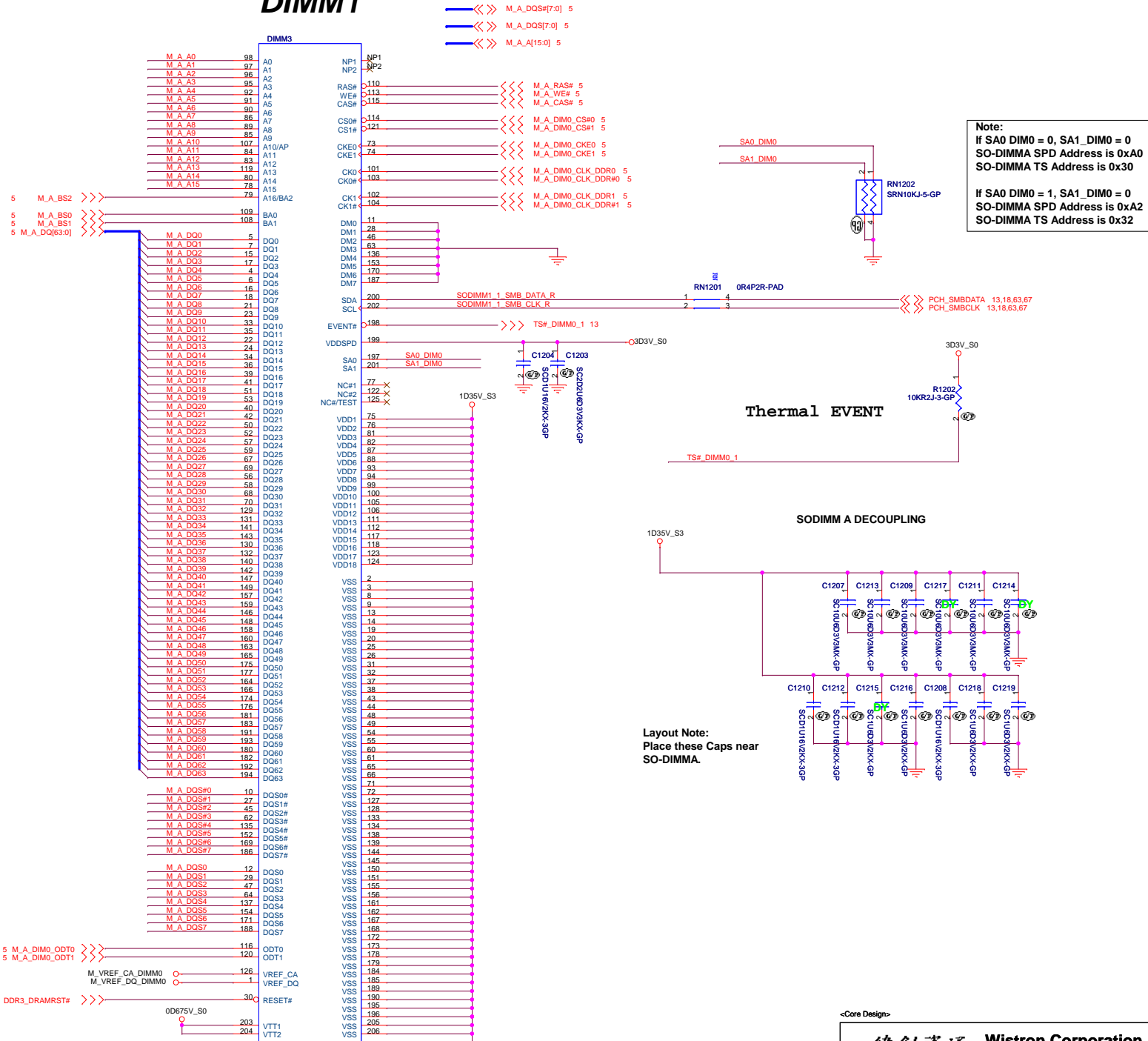
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| | | | |
|------------------|---|----------|----------|
| Title | | | |
| CPU (VSS) | | | |
| Size | Document Number | Rev | |
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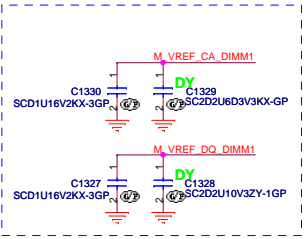
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DIMM1

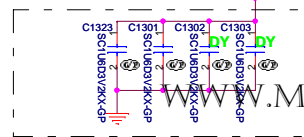


5 M_B_A[15:0] <<>>
 5 M_B_DQS#7[0] <<>>
 5 M_B_DQS#7[0] <<>>

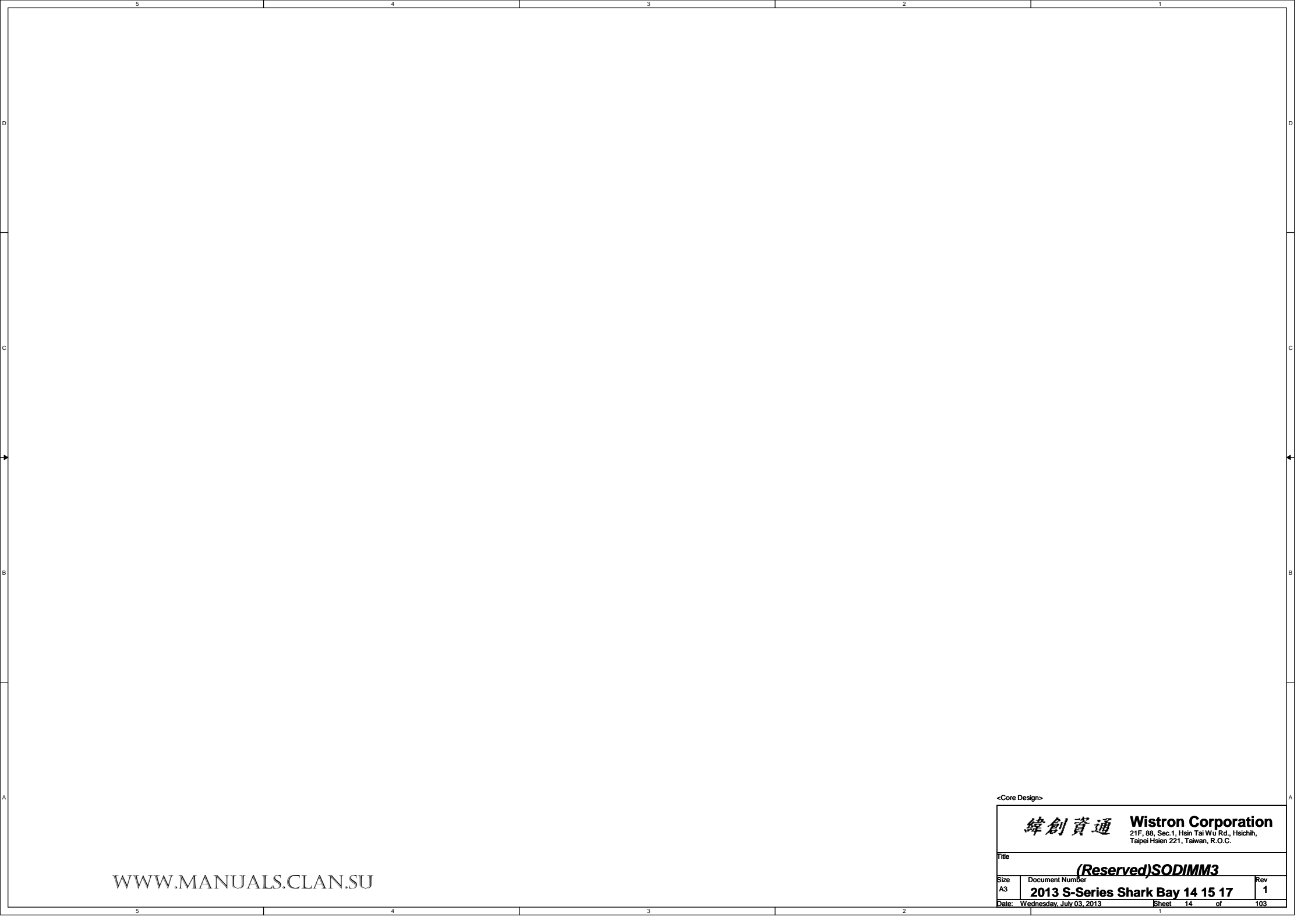
5 M_B_BS2 >>>>
 5 M_B_BS0 >>>>
 5 M_B_BS1 >>>>
 5 M_B_DQ[63:0] >>>>



Place these caps close to VTT1 and VTT2.



| | | |
|----------|-----|---------|
| M_B_A0 | 98 | A0 |
| M_B_A1 | 97 | A1 |
| M_B_A2 | 96 | A2 |
| M_B_A3 | 95 | A3 |
| M_B_A4 | 92 | A4 |
| M_B_A5 | 91 | A5 |
| M_B_A6 | 90 | A6 |
| M_B_A7 | 86 | A7 |
| M_B_A8 | 89 | A8 |
| M_B_A9 | 89 | A9 |
| M_B_A10 | 107 | A10/AP |
| M_B_A11 | 84 | A11 |
| M_B_A12 | 83 | A12 |
| M_B_A13 | 119 | A13 |
| M_B_A14 | 80 | A14 |
| M_B_A15 | 78 | A15 |
| | 79 | A16/BA2 |
| | 109 | BA0 |
| | 108 | BA1 |
| M_B_DQ0 | 5 | DQ0 |
| M_B_DQ1 | 7 | DQ1 |
| M_B_DQ2 | 15 | DQ2 |
| M_B_DQ3 | 17 | DQ3 |
| M_B_DQ4 | 4 | DQ4 |
| M_B_DQ5 | 6 | DQ5 |
| M_B_DQ6 | 16 | DQ6 |
| M_B_DQ7 | 18 | DQ7 |
| M_B_DQ8 | 21 | DQ8 |
| M_B_DQ9 | 23 | DQ9 |
| M_B_DQ10 | 33 | DQ10 |
| M_B_DQ11 | 36 | DQ11 |
| M_B_DQ12 | 22 | DQ12 |
| M_B_DQ13 | 24 | DQ13 |
| M_B_DQ14 | 34 | DQ14 |
| M_B_DQ15 | 36 | DQ15 |
| M_B_DQ16 | 39 | DQ16 |
| M_B_DQ17 | 41 | DQ17 |
| M_B_DQ18 | 51 | DQ18 |
| M_B_DQ19 | 53 | DQ19 |
| M_B_DQ20 | 40 | DQ20 |
| M_B_DQ21 | 50 | DQ21 |
| M_B_DQ22 | 50 | DQ22 |
| M_B_DQ23 | 52 | DQ23 |
| M_B_DQ24 | 57 | DQ24 |
| M_B_DQ25 | 59 | DQ25 |
| M_B_DQ26 | 67 | DQ26 |
| M_B_DQ27 | 69 | DQ27 |
| M_B_DQ28 | 56 | DQ28 |
| M_B_DQ29 | 58 | DQ29 |
| M_B_DQ30 | 68 | DQ30 |
| M_B_DQ31 | 70 | DQ31 |
| M_B_DQ32 | 129 | DQ32 |
| M_B_DQ33 | 131 | DQ33 |
| M_B_DQ34 | 141 | DQ34 |
| M_B_DQ35 | 143 | DQ35 |
| M_B_DQ36 | 130 | DQ36 |
| M_B_DQ37 | 132 | DQ37 |
| M_B_DQ38 | 140 | DQ38 |
| M_B_DQ39 | 142 | DQ39 |
| M_B_DQ40 | 147 | DQ40 |
| M_B_DQ41 | 149 | DQ41 |
| M_B_DQ42 | 157 | DQ42 |
| M_B_DQ43 | 159 | DQ43 |
| M_B_DQ44 | 146 | DQ44 |
| M_B_DQ45 | 148 | DQ45 |
| M_B_DQ46 | 158 | DQ46 |
| M_B_DQ47 | 160 | DQ47 |
| M_B_DQ48 | 163 | DQ48 |
| M_B_DQ49 | 165 | DQ49 |
| M_B_DQ50 | 175 | DQ50 |
| M_B_DQ51 | 177 | DQ51 |
| M_B_DQ52 | 164 | DQ52 |
| M_B_DQ53 | 166 | DQ53 |
| M_B_DQ54 | 174 | DQ54 |
| M_B_DQ55 | 176 | DQ55 |
| M_B_DQ56 | 181 | DQ56 |
| M_B_DQ57 | 183 | DQ57 |
| M_B_DQ58 | 191 | DQ58 |
| M_B_DQ59 | 193 | DQ59 |
| M_B_DQ60 | 180 | DQ60 |
| M_B_DQ61 | 182 | DQ61 |
| M_B_DQ62 | 192 | DQ62 |
| M_B_DQ63 | 194 | DQ63 |



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Title

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Size
A3

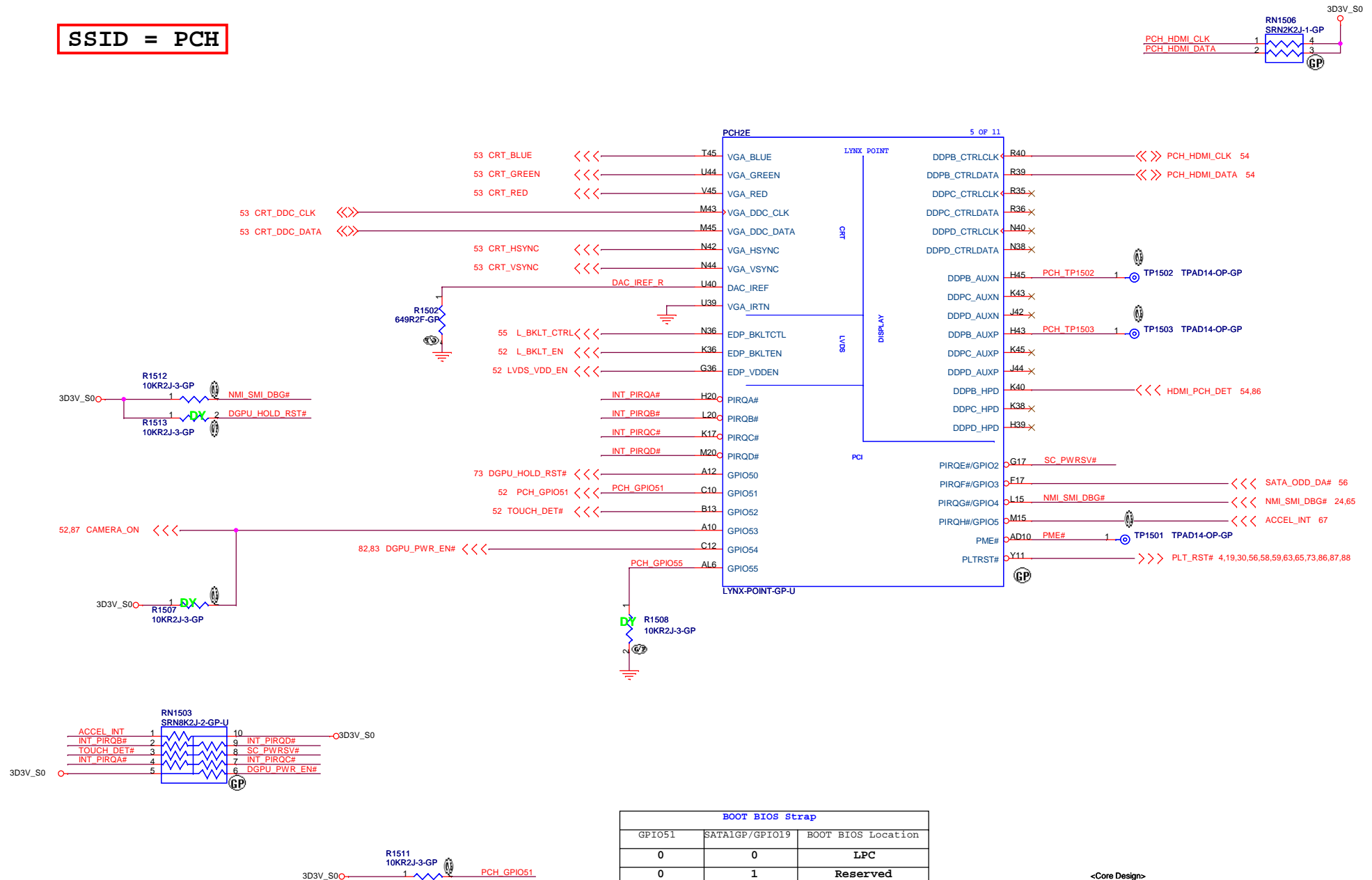
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SSID = PCH



| BOOT BIOS Strap | | |
|-----------------|----------------|--------------------|
| GPIO51 | SATA1GP/GPIO19 | BOOT BIOS Location |
| 0 | 0 | LPC |
| 0 | 1 | Reserved |
| 1 | 0 | Reserved |
| 1 | 1 | SPI(Default) |

<Core Design>

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Title

PCH (PCI/CRT/DDI)

Size
A3

Document Number
2013 E-So

2013 S-Series Shark Bay 14 15 17

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| Rev |
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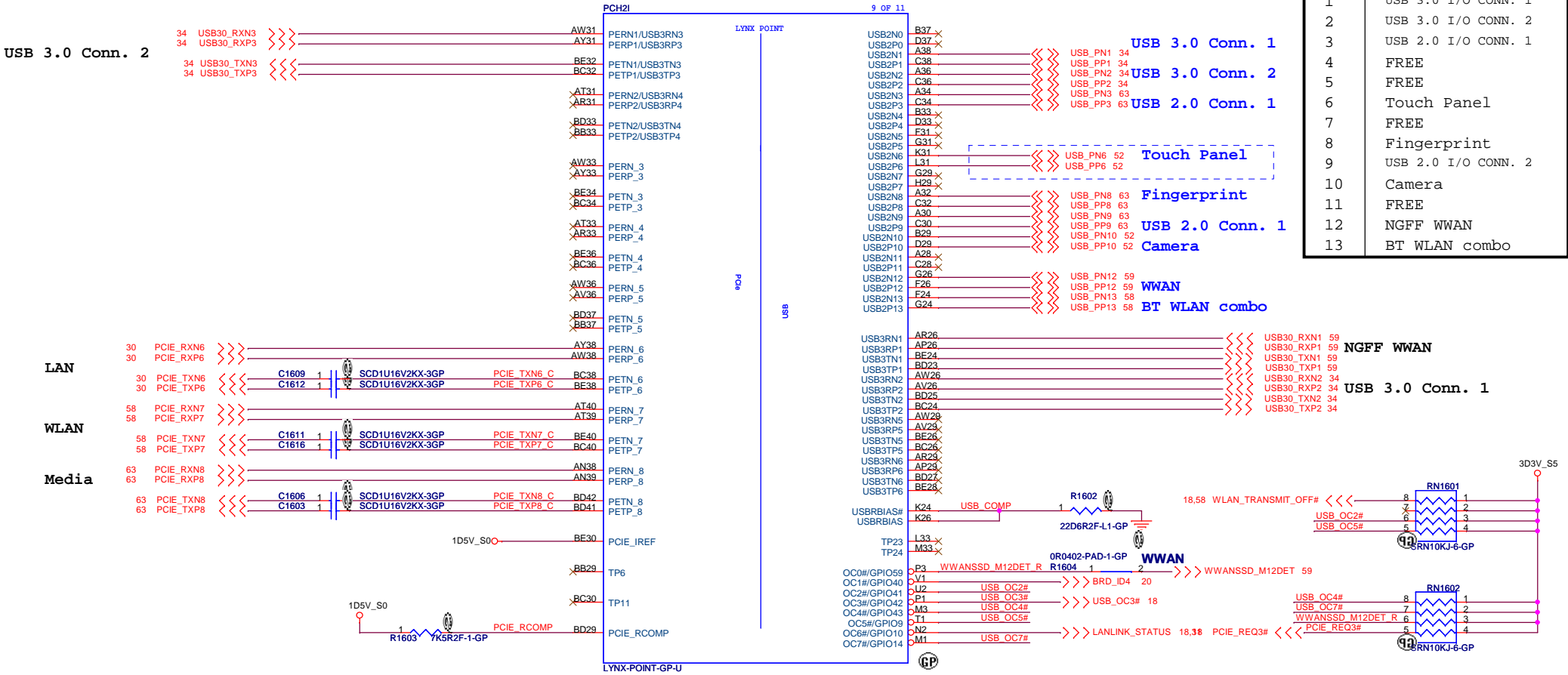
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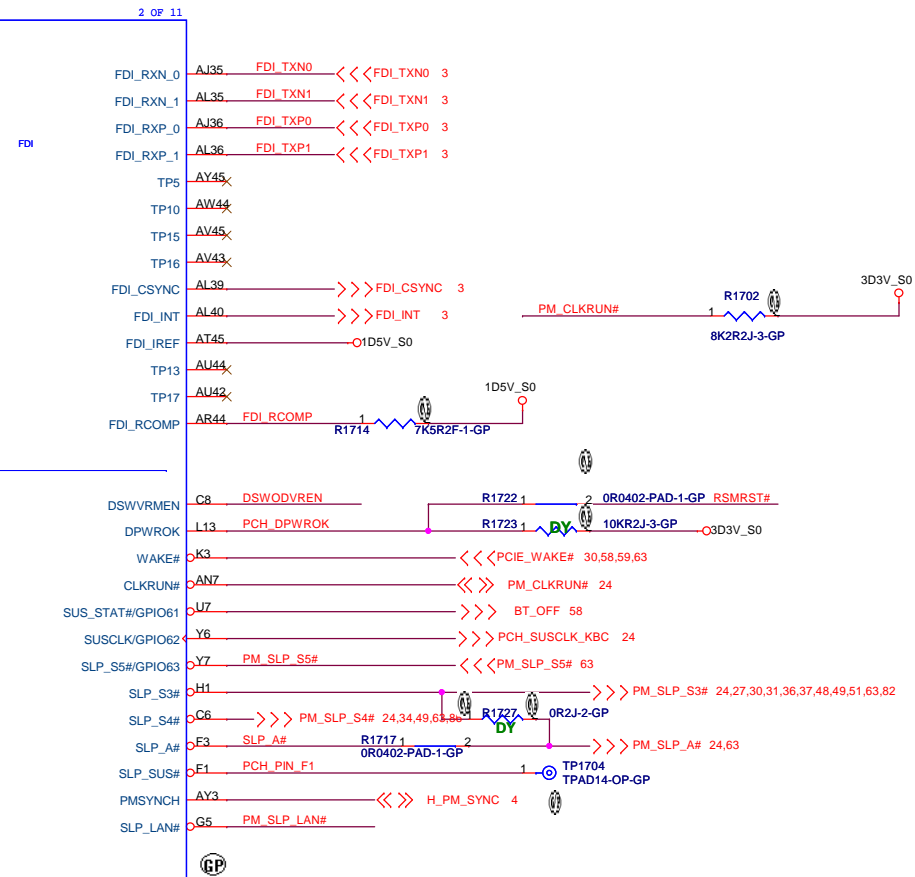
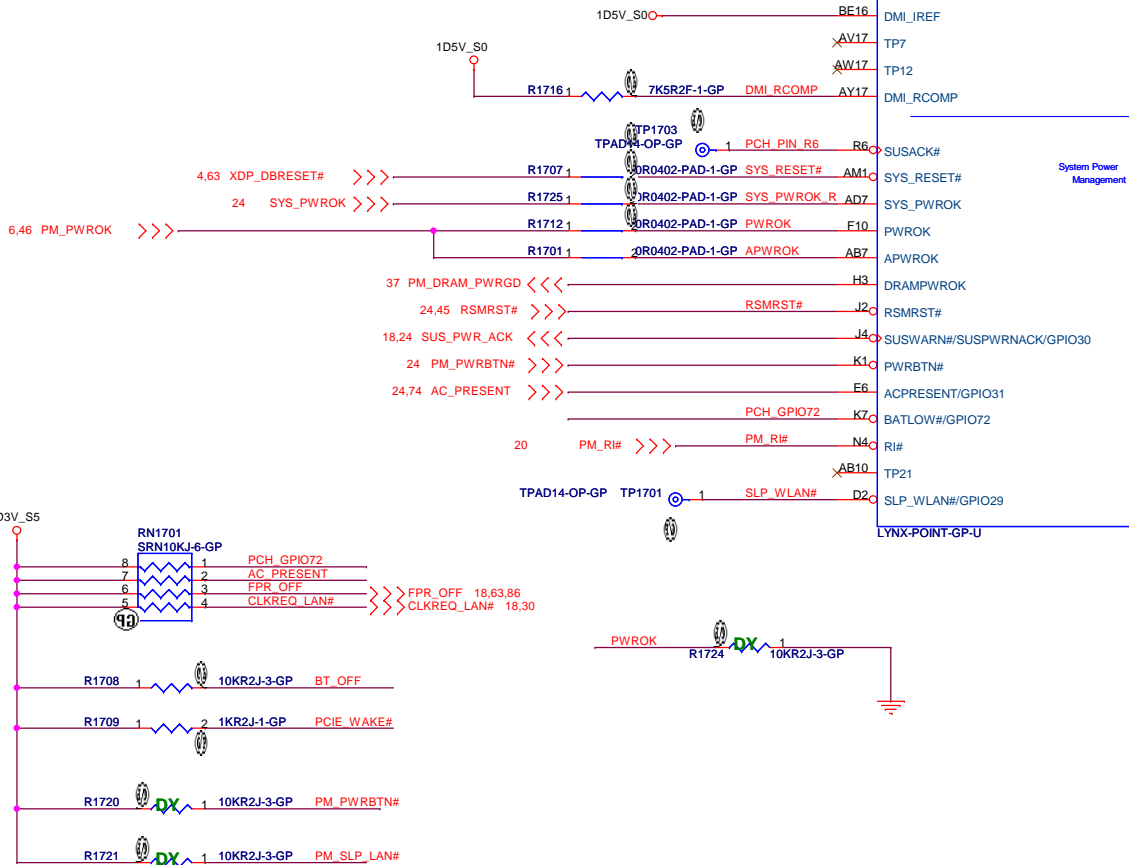
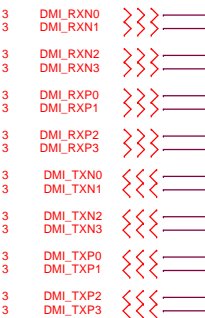
SSID = PCH

USB2.0 Table

| USB | |
|------|---------------------|
| Pair | Device |
| 0 | FREE |
| 1 | USB 3.0 I/O CONN. 1 |
| 2 | USB 3.0 I/O CONN. 2 |
| 3 | USB 2.0 I/O CONN. 1 |
| 4 | FREE |
| 5 | FREE |
| 6 | Touch Panel |
| 7 | FREE |
| 8 | Fingerprint |
| 9 | USB 2.0 I/O CONN. 2 |
| 10 | Camera |
| 11 | FREE |
| 12 | NGFF WWAN |
| 13 | BT WLAN combo |



SSID = PCH



| | |
|----------------------------------|-------------------|
| DSWODVREN - On Die DSW VR Enable | |
| HIGH | Enabled (DEFAULT) |
| LOW | Disabled |

The diagram illustrates the electrical connection for the DSWODVREN signal. A red line labeled DSWODVREN enters from the left. It splits into two parallel paths. The upper path contains a resistor labeled R1703 in series with a diode labeled 330KR2J-1-GP. The lower path contains a resistor labeled R1704 in series with a diode labeled 330KR2J-1-GP. Both paths converge and connect to a terminal labeled RTC_AUX_S1. A ground symbol is shown at the bottom right.

<Core Design>

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Title

PCH (DMI/FDI/PM)

Size

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| Document Number | |
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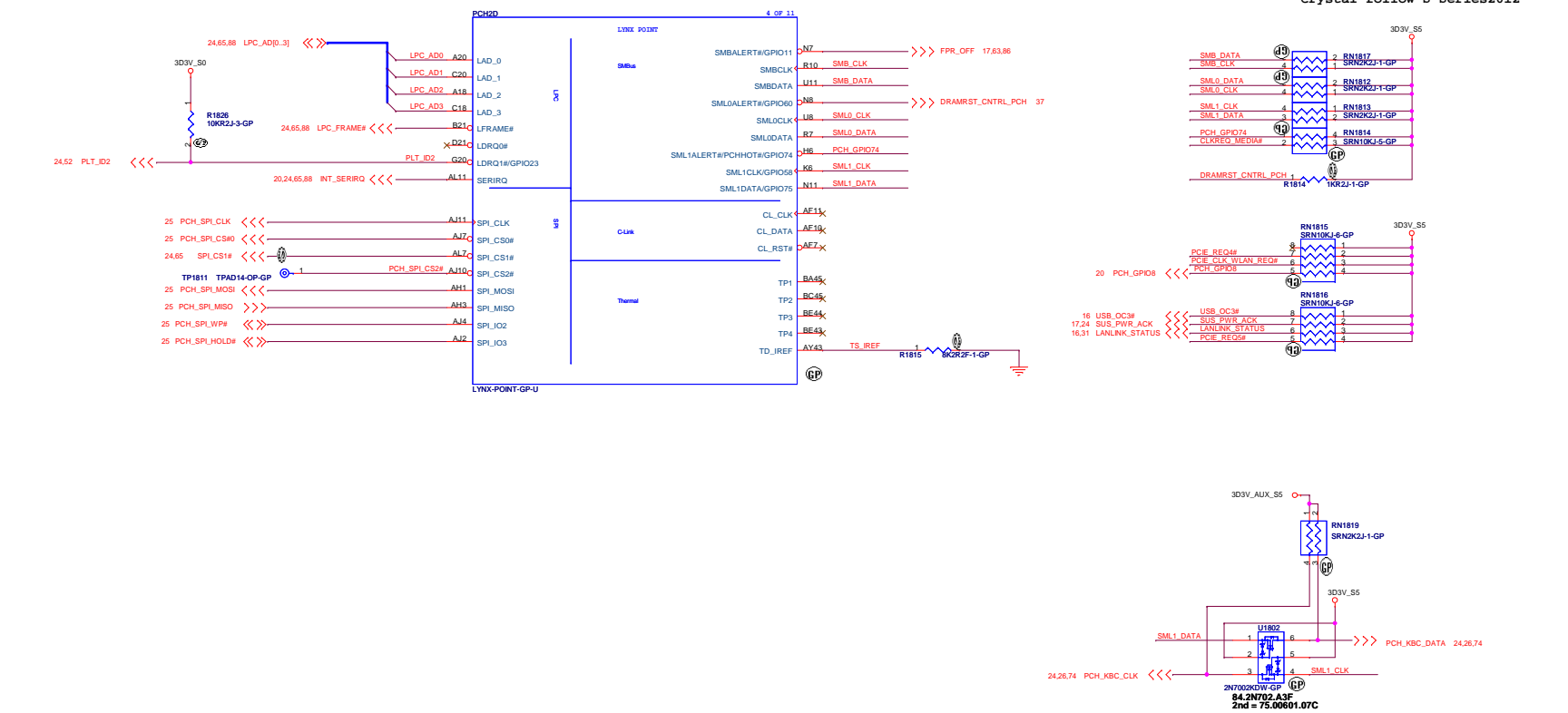
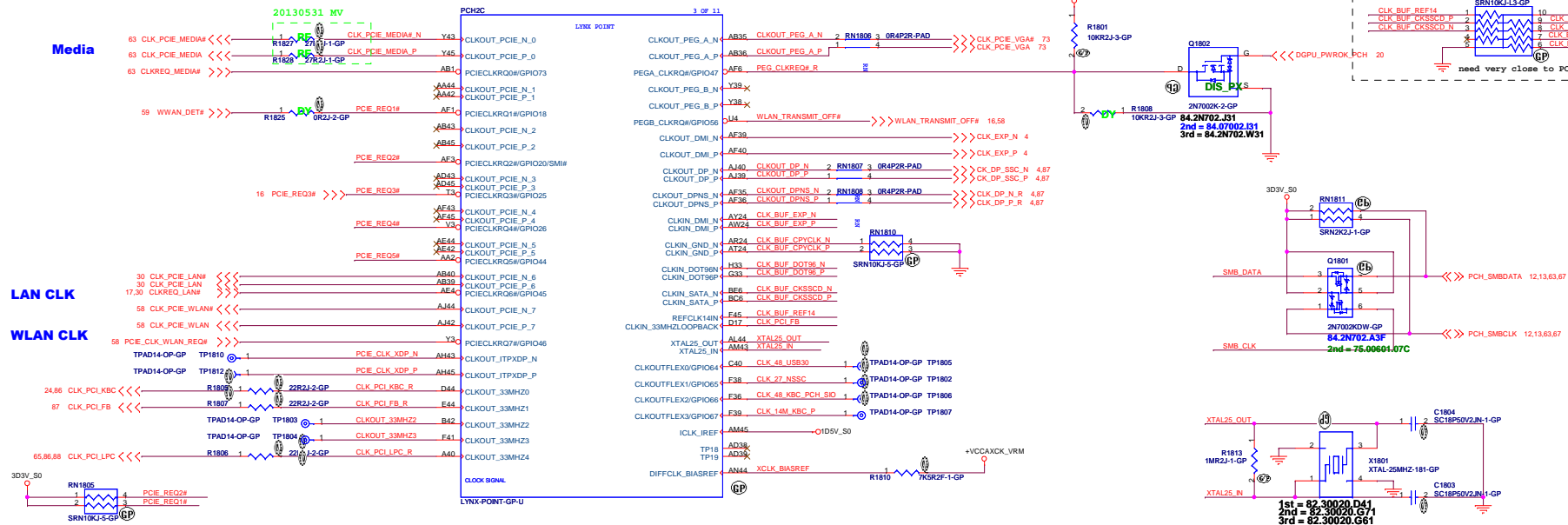
Rev

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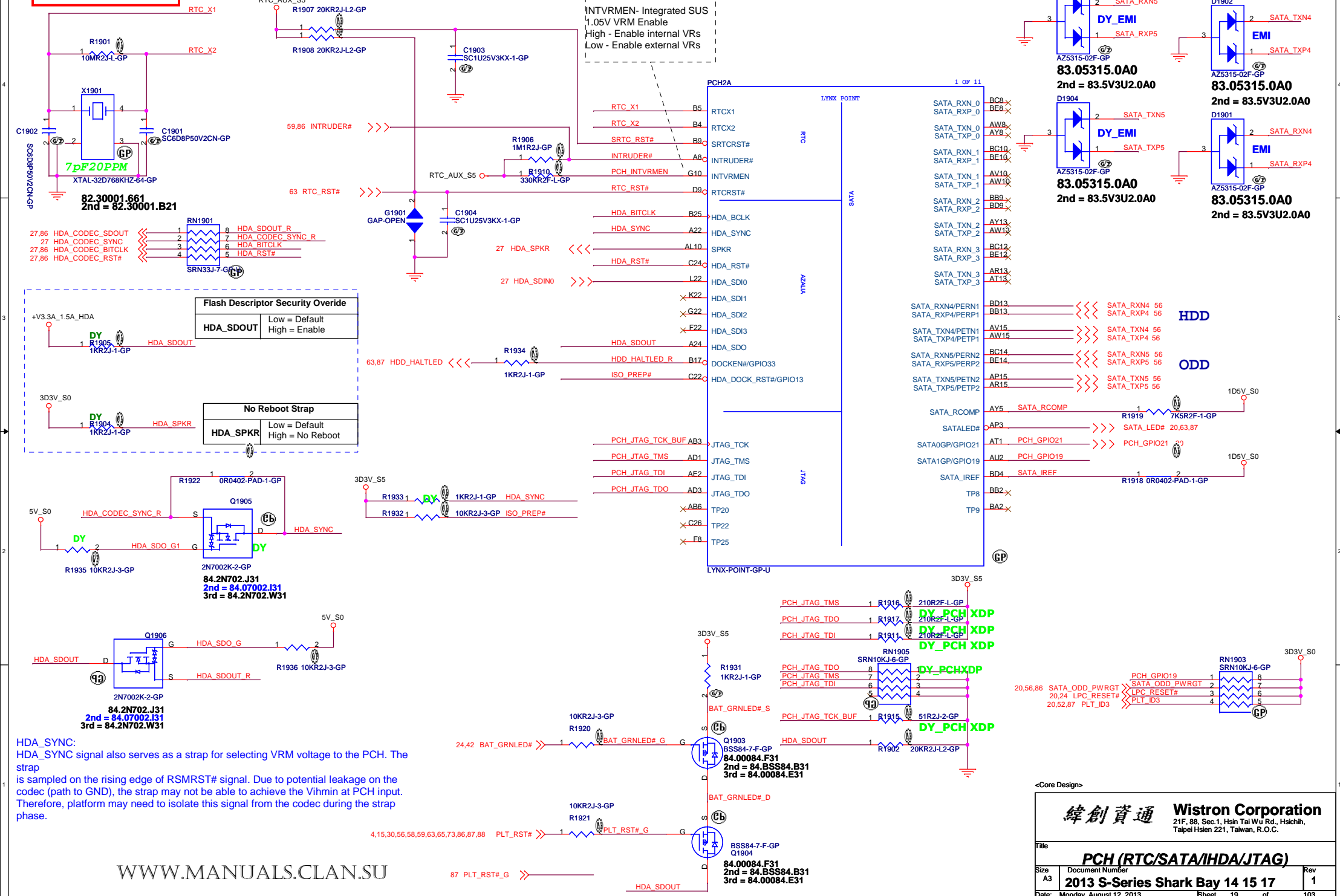
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WWW.MANUALS.CLAN.SU

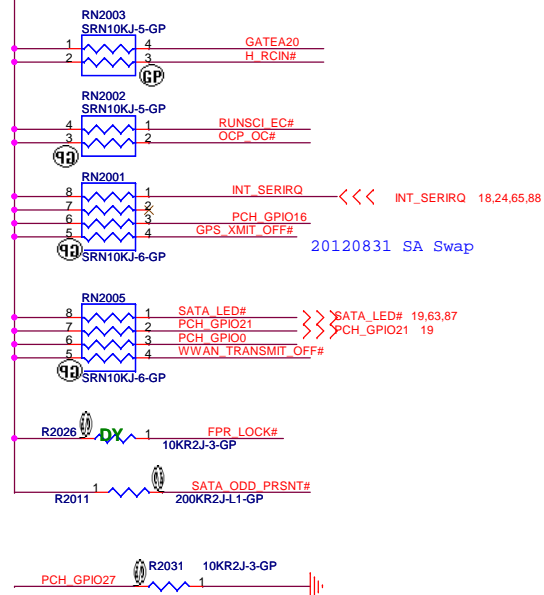
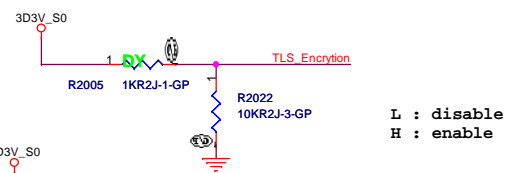
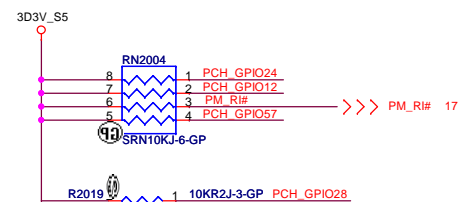
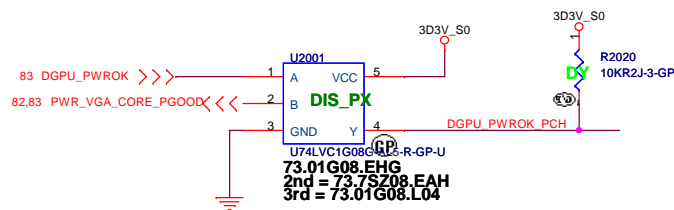
SSID = PCH



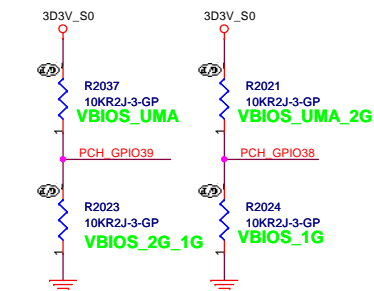
SSID = PCH



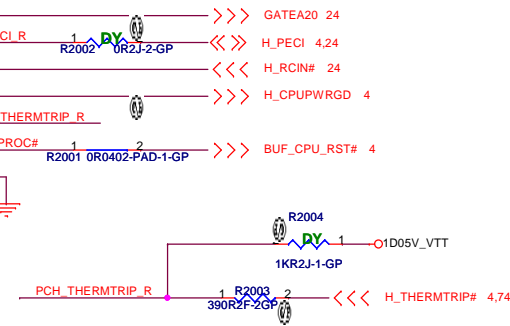
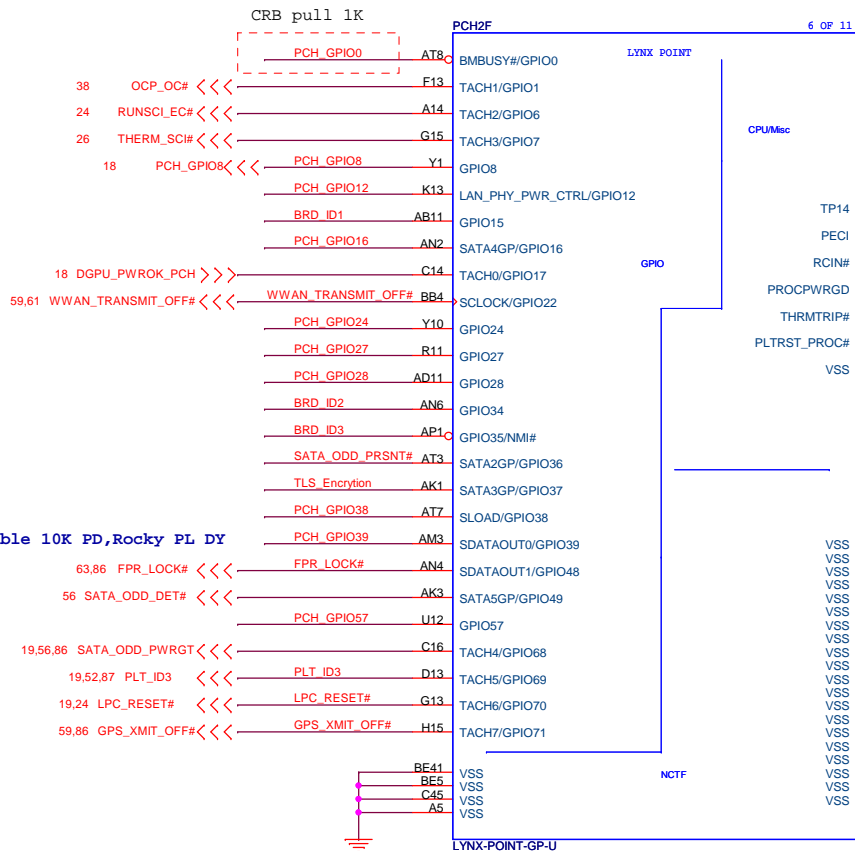
SSID = PCH



VBIOS ID TABLE



| PCH_GPIO39 | PCH_GPIO38 | |
|------------|------------|---------|
| 0 | 1 | 128MX16 |
| 1 | 0 | N/A |
| 1 | 1 | UMA |
| 0 | 0 | 64MX16 |



| | BRD_ID1 | BRD_ID2 | BRD_ID3 | BRD_ID4 |
|--------|---------|---------|---------|---------|
| GPIO15 | GPIO34 | GPIO35 | GPIO40 | |
| DB 0 | 0 | 0 | 0 | 0 |
| DB 1 | 0 | 0 | 0 | 1 |
| DB 2 | 0 | 0 | 1 | 0 |
| | 0 | 0 | 1 | 1 |
| SI 1 | 0 | 1 | 0 | 0 |
| SI 1B | 0 | 1 | 0 | 1 |
| SI 2 | 0 | 1 | 1 | 0 |
| | 0 | 1 | 1 | 1 |
| PV 1 | 1 | 0 | 0 | 0 |
| | 1 | 0 | 0 | 1 |
| | 1 | 0 | 1 | 0 |
| | 1 | 0 | 1 | 1 |
| MV | 1 | 1 | 0 | 0 |
| | 1 | 1 | 0 | 1 |
| | 1 | 1 | 1 | 0 |
| | 1 | 1 | 1 | 1 |

<Core Design>

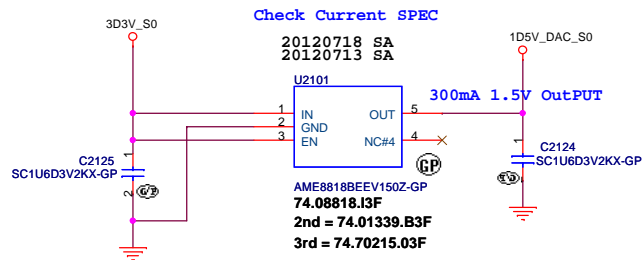
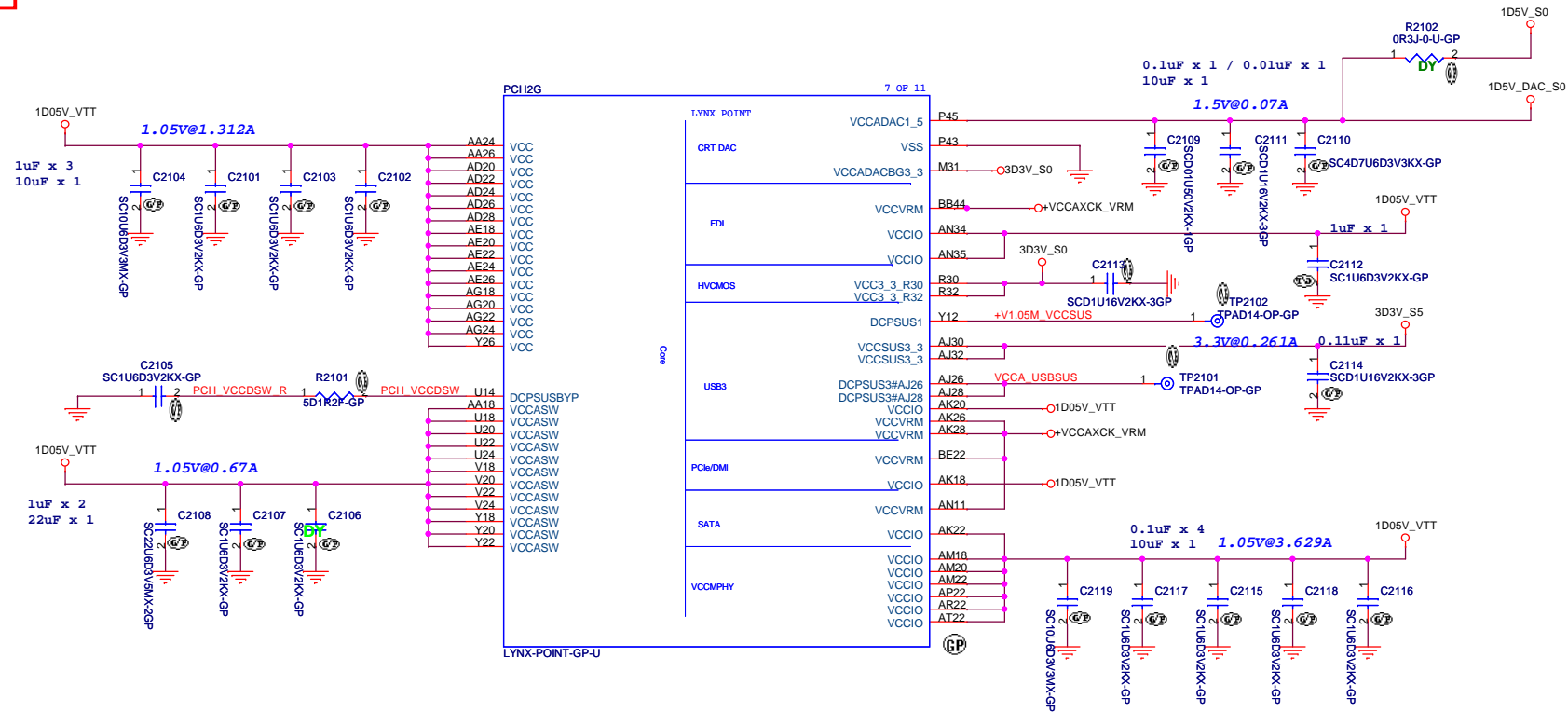
緯創資通 Wistron Corporation
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Taipei Hsein 221, Taiwan, R.O.C.

File: PCH (GPIO/CPU)

Size: A3 Document Number: 2013 S-Series Shark Bay 14 15 17 Rev: 1

Date: Monday, August 12, 2013 Sheet: 20 of 103

SSID = PCH

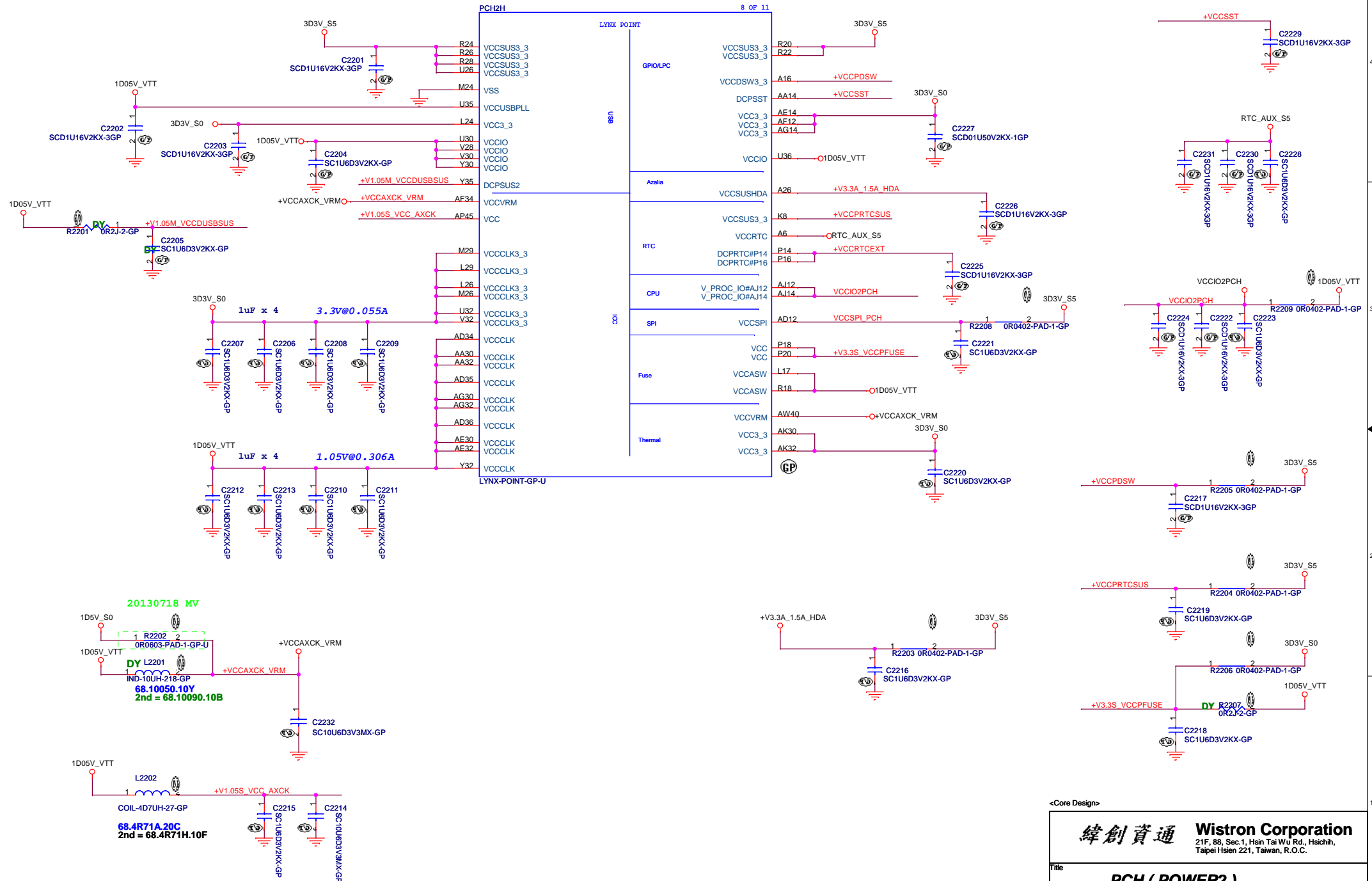


<Core Design>

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| | | | | |
|-------|----------------------------------|-------|---------------|--------|
| Title | | | PCH (POWER1) | |
| Size | Document Number | Rev | | |
| A3 | 2013 S-Series Shark Bay 14 15 17 | 1 | | |
| Date: | Wednesday, July 24, 2013 | Sheet | 21 | of 103 |

SSID = PCH



<Core Design>

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Title

PCH (POWER2)

Size

| | |
|-----------------|--|
| Document Number | |
|-----------------|--|

2013 S-Series Shark Bay 14 15 17

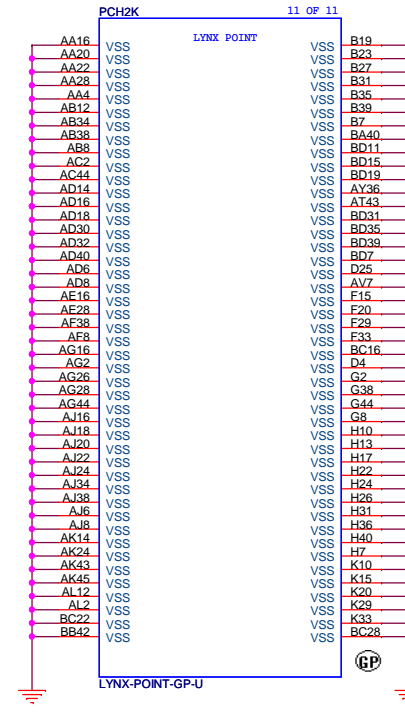
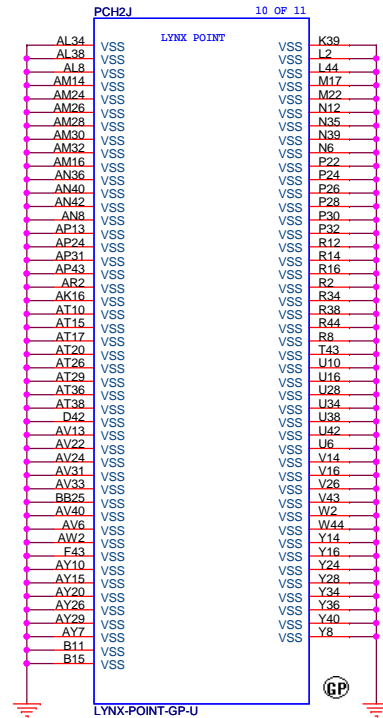
Rev

Date: Wednesday, July 24, 2013

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WWW.MANUALS.CLAN.SU

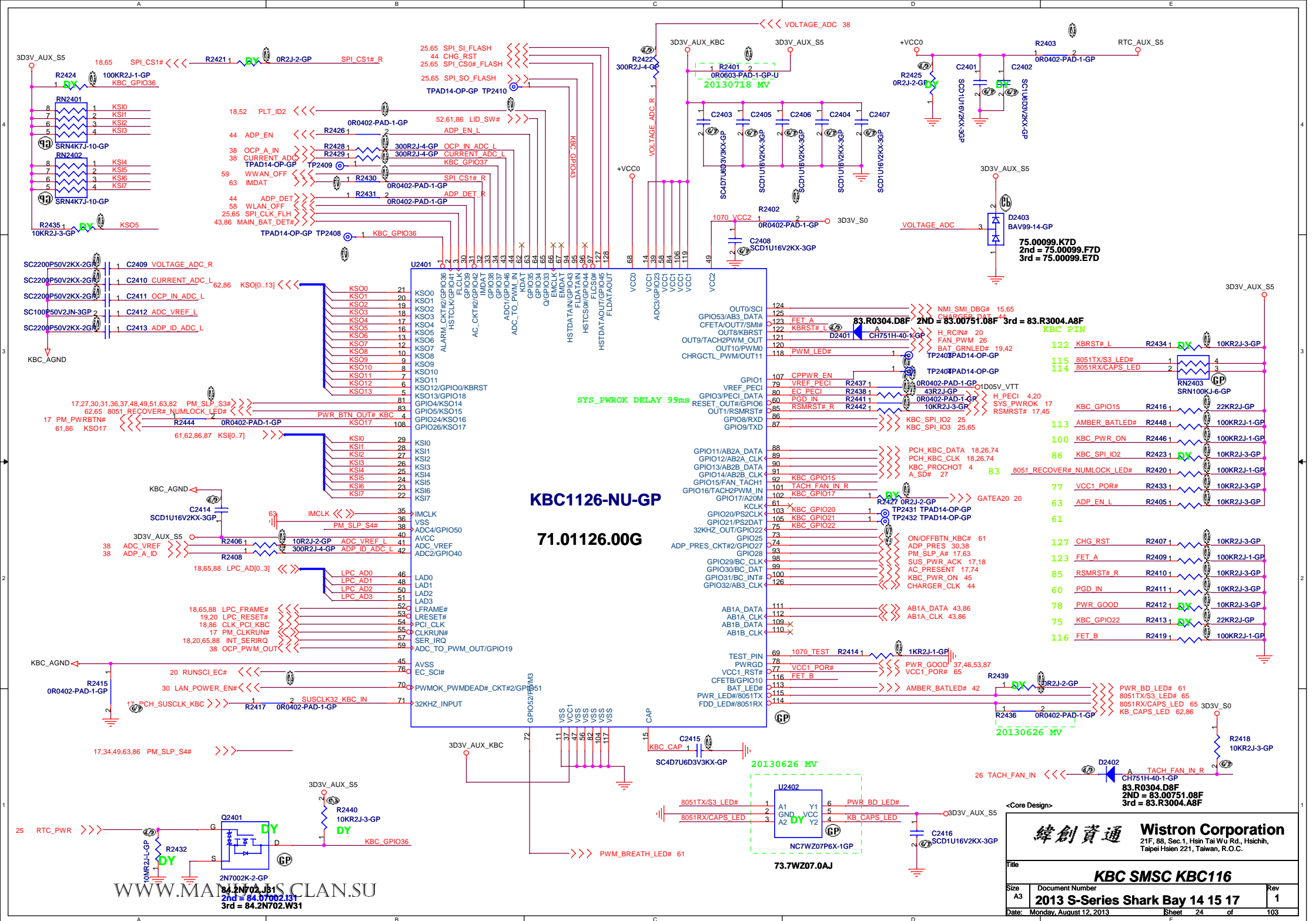
SSID = PCH



<Core Design>

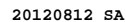
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

| | | | |
|-------|----------------------------------|-------|-----------|
| Title | | | PCH(VSS) |
| Size | Document Number | Rev | |
| A3 | 2013 S-Series Shark Bay 14 15 17 | 1 | |
| Date: | Wednesday, July 03, 2013 | Sheet | 23 of 103 |

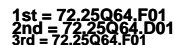


To PCH

From BIOS



TO RF CAP

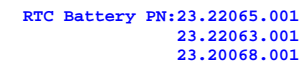
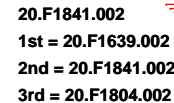


NOTE: SPI signal use GND reference

```
Quad IO Winbond 8M:72.25Q64.K01 ( W25Q64FVSSIQ )
      MXIC :   72.25647.00A ( MX25L6473EM2I )
      Micon:  72.25Q64.G01 ( N25Q064A13ESEC0F )
```

WWW.MANUALS.CLAN.SU

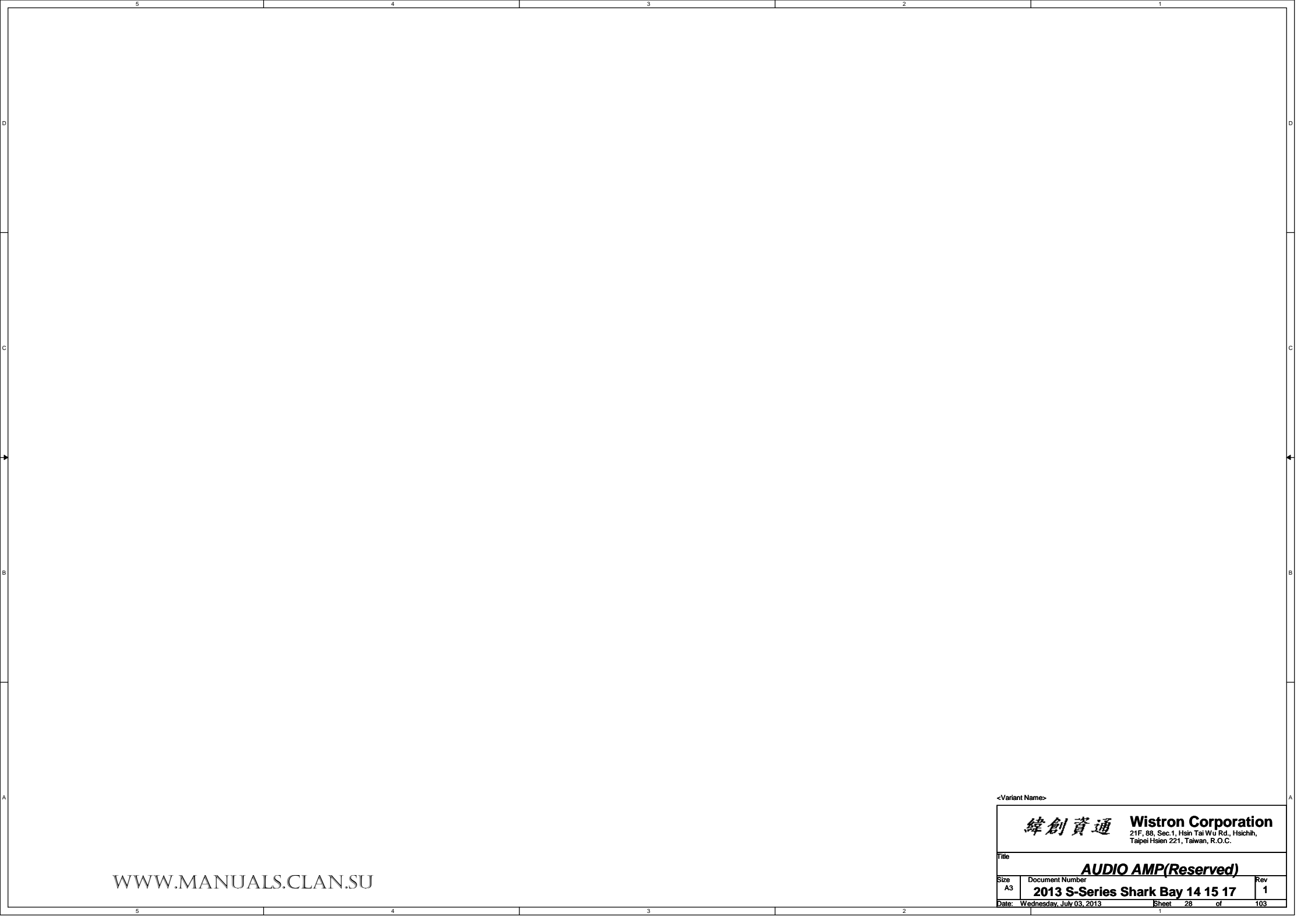
RTC Battery+Cable
PN:23.21212.033
2nd=23.21221.023



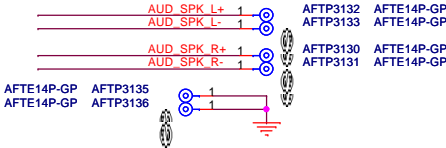
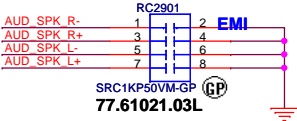
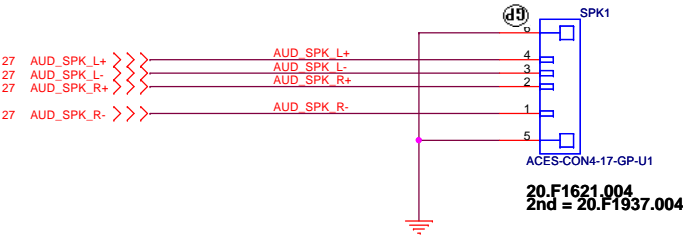
<Core Design>

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| | | | |
|---------------------------|---|----------|-----------|
| Title | | | |
| Flash(KBC+PCH)/RTC | | | |
| Size | Document Number | Rev | |
| A3 | 2013 S-Series Shark Bay 14 15 17 | 1 | |
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Speaker Connector



LAN RJ45

USE EFuse No ASF

DEL

LAN CHIP-RTL8151GH

Regout power plane(1D05V)

LanChip Power

+3.3V_LAN_S5 Rising time
(10%~90%)
Spec >1ms and <100ms

cap near pin11,32 <200mils

C3026 to C3012

Remove R3003

C3001 to C3017

60 mils (average 300mA)

20130718 MV

20130805 MV

Put 4D7U L + 4D7U cap near pin24 <200mils
(2nd = 78.22610.81L)

Lan Power Inductance Spec
(1) IDC >= 600mA
(2) Tolerance < 20%
(3) RDC <= 0.8ohms(Max)
(4) Efficiency >= 80%

Regout Switch

EEPROM LED OPTION USE '00'
=> LED0 : ACT (Amber)
=> LED1 : LINK (White)
(BOTH 10/100 & GIGA CHIP)
(Power down => Kept high)

| | |
|----|-----------|
| DB | RTL8151GH |
| SI | RTL8151GH |

RTL8161GSH
Install:L3003 C3030 C3031 C3026 C3001
DY:R3007

25MHz Crystal

1st = 82.30020.D41
2nd = 82.30020.G71
3rd = 82.30020.G61

Isolate Strap Pin

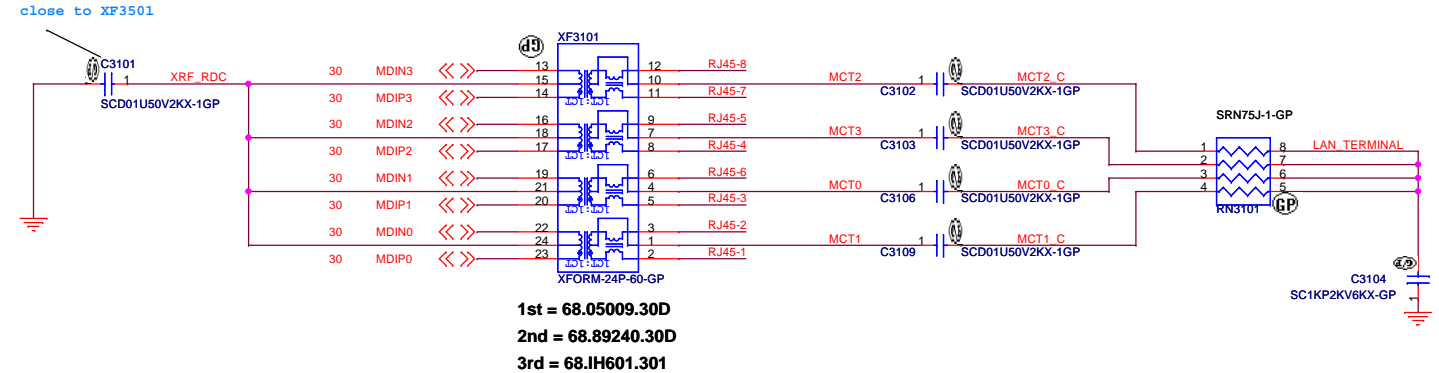
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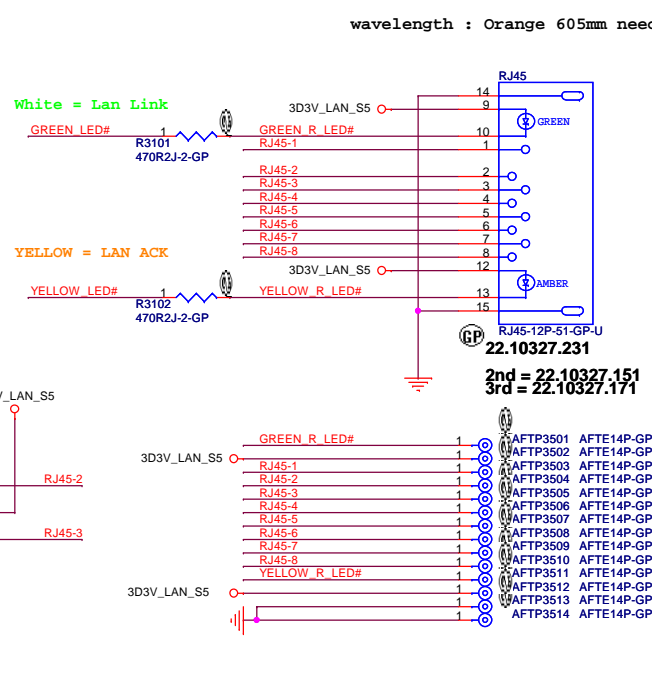
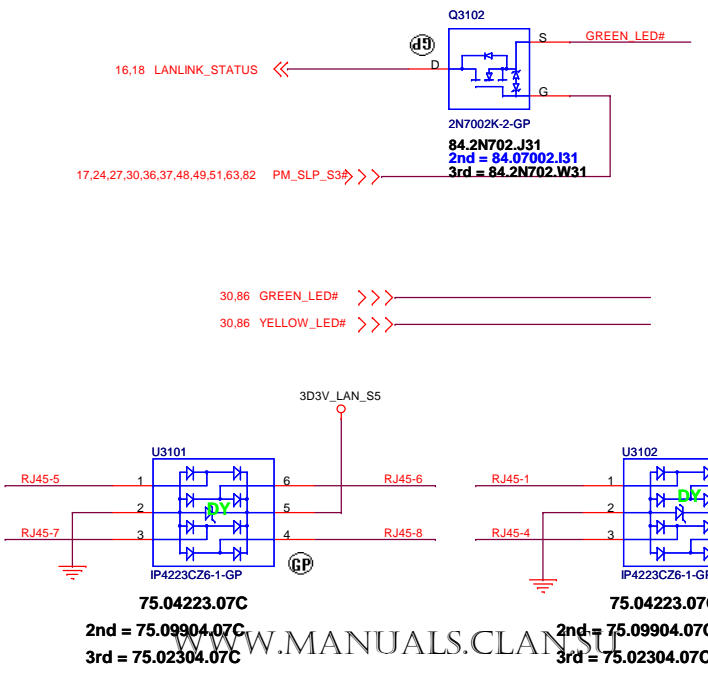
Title Lan Realtek 8151GH

| | | |
|-------------------------------|--|--------|
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| Date: Monday, August 12, 2013 | Sheet 30 | of 103 |

White LED for connectivity and Amber LED for activity located on RJ-45 connector



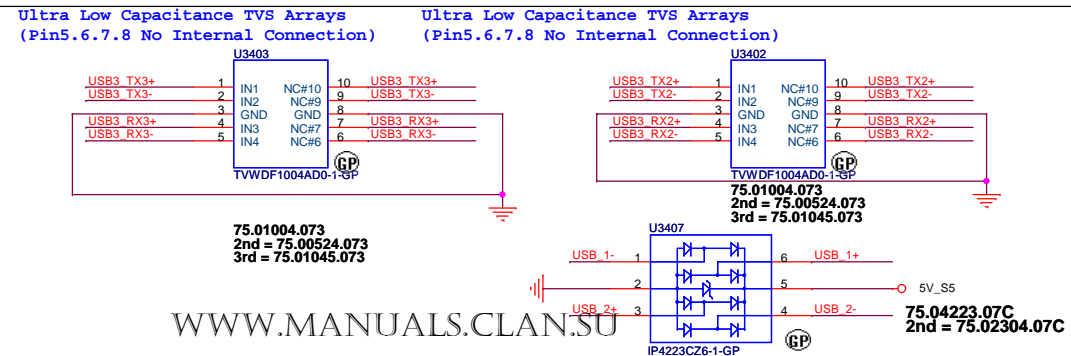
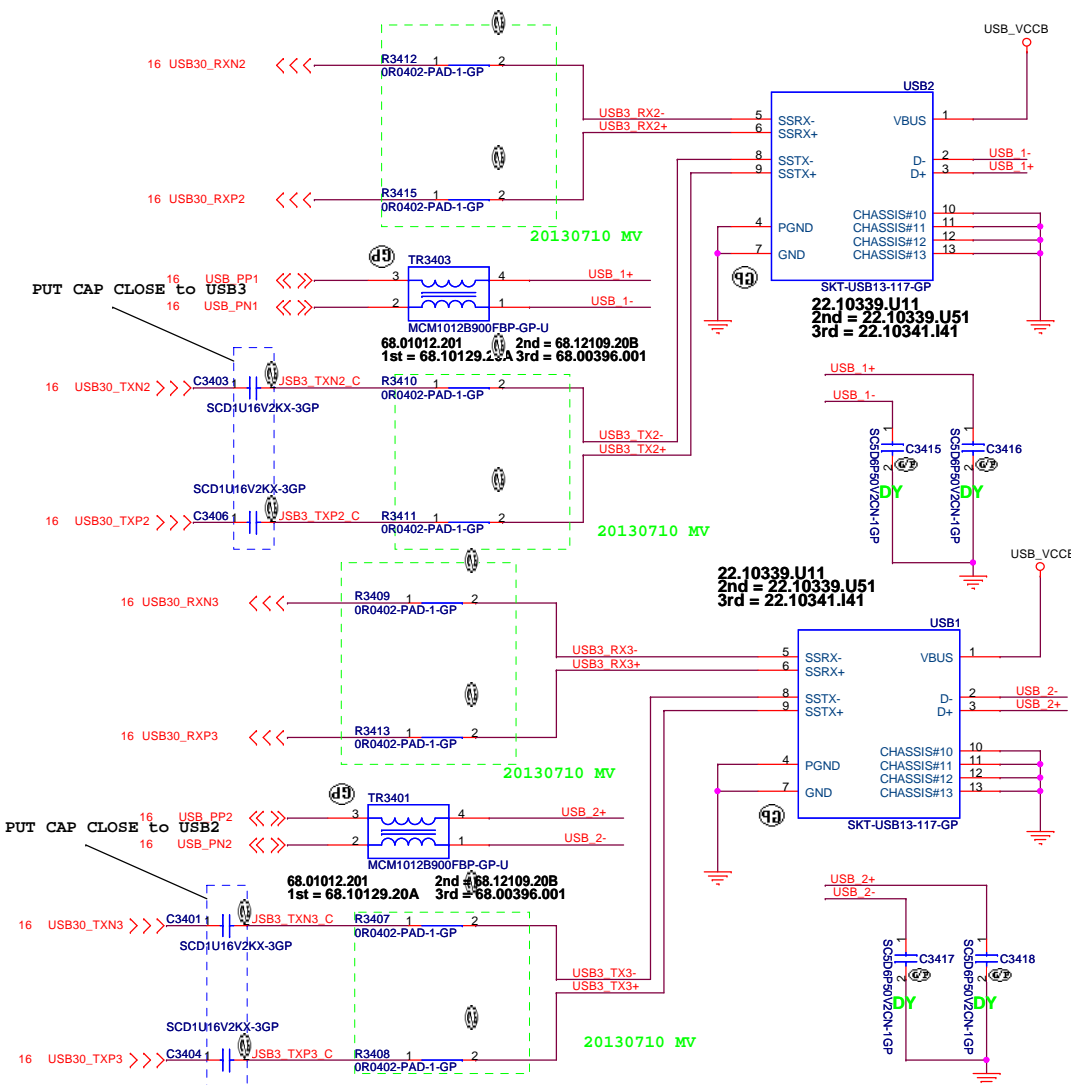
RJ45 Connector



- (1) route on bottom as differential pairs.
- (2) Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- (3) No vias, No 90 degree bends.
- (4) pairs must be equal lengths.
- (5) 6mil trace width, 12mil separation.
- (6) 36mil between pairs and any other trace.
- (7) Must not cross ground moat, except RJ-45 moat.



Left Side USB 3.0 Connector



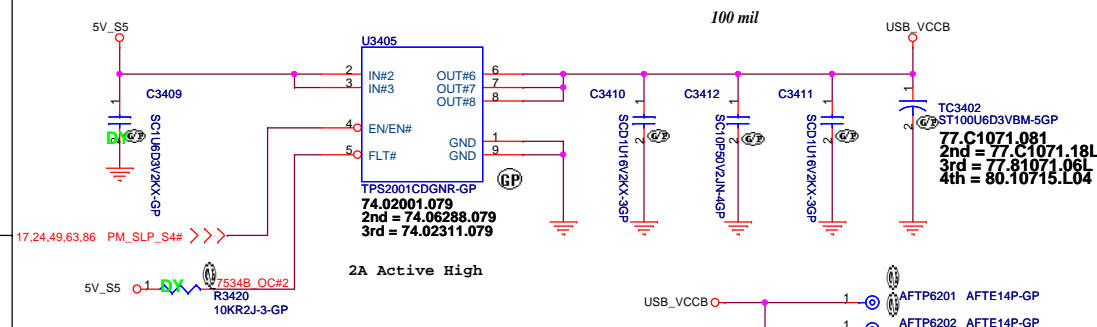
USB 3.0 Connector Pin definition

| Pin | Definition |
|-----|------------|
| 1 | POWER |
| 2 | USB 2.0 D- |
| 3 | USB 2.0 D+ |
| 4 | GND |
| 5 | StdA_SSRX- |
| 6 | StdA_SSRX+ |
| 7 | GND |
| 8 | StdA_SSTX- |
| 9 | StdA_SSTX+ |

USB 3.0/2.0 Port Pairing

| USB3.0 | USB2.0 |
|--------|--------|
| Port 1 | Port 0 |
| Port 2 | Port 1 |
| Port 3 | Port 2 |
| Port 4 | Port 3 |
| Port 5 | Port 4 |
| Port 6 | Port 5 |

USB POWER



<Core Design>

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| | | |
|-------------------|----------------------------------|-----------------|
| Title | | |
| USB 2.0/ 3.0 Port | | |
| Size | Document Number | Rev |
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| | | | | | |
|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | |
| C | | | | | |
| B | | | | | |
| A | | | | | |

<Core Design>

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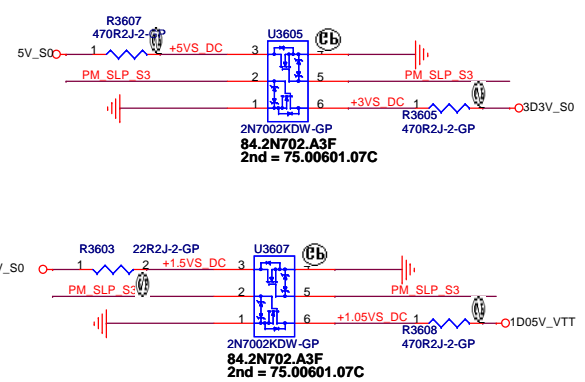
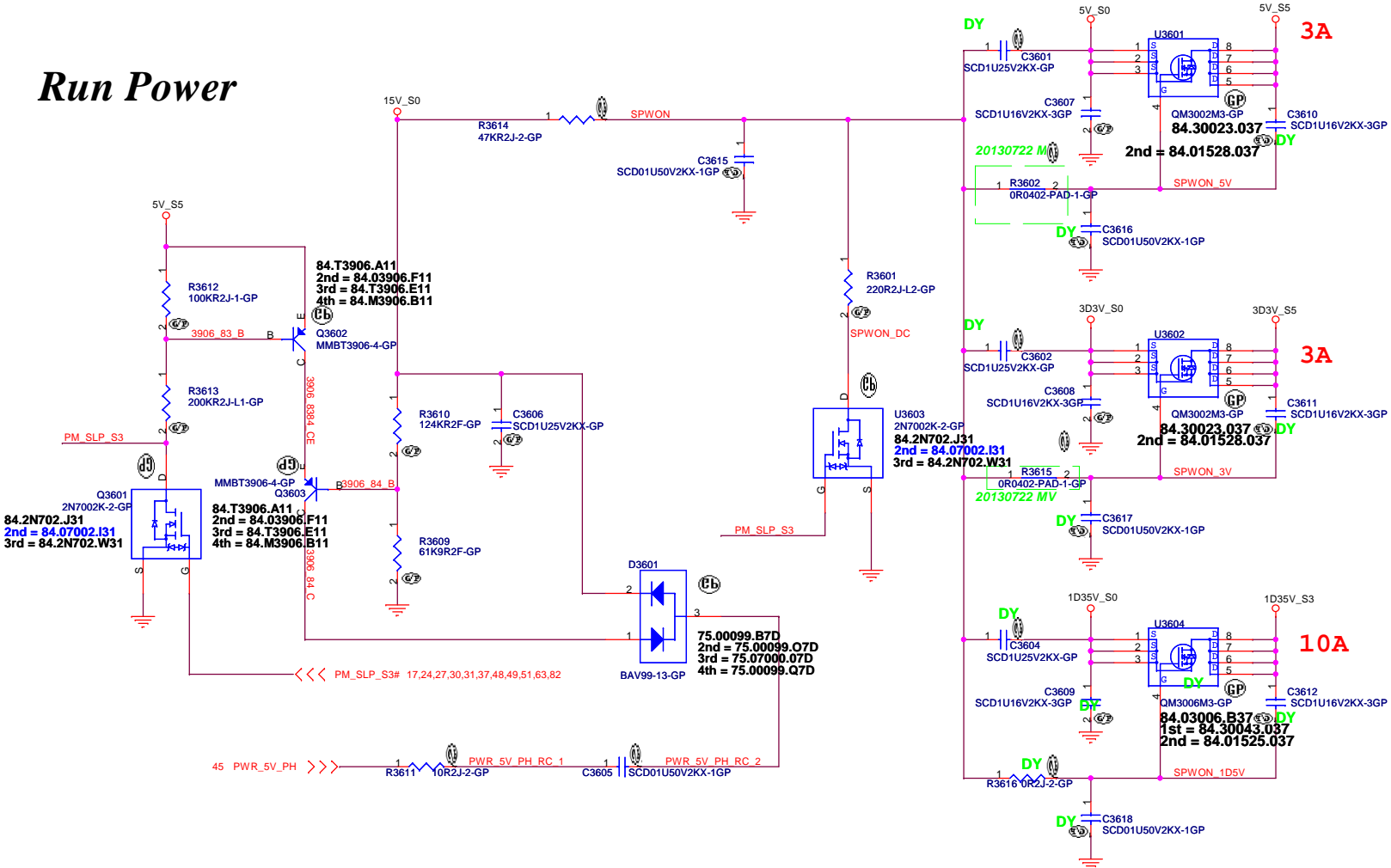
Title

USB Charger

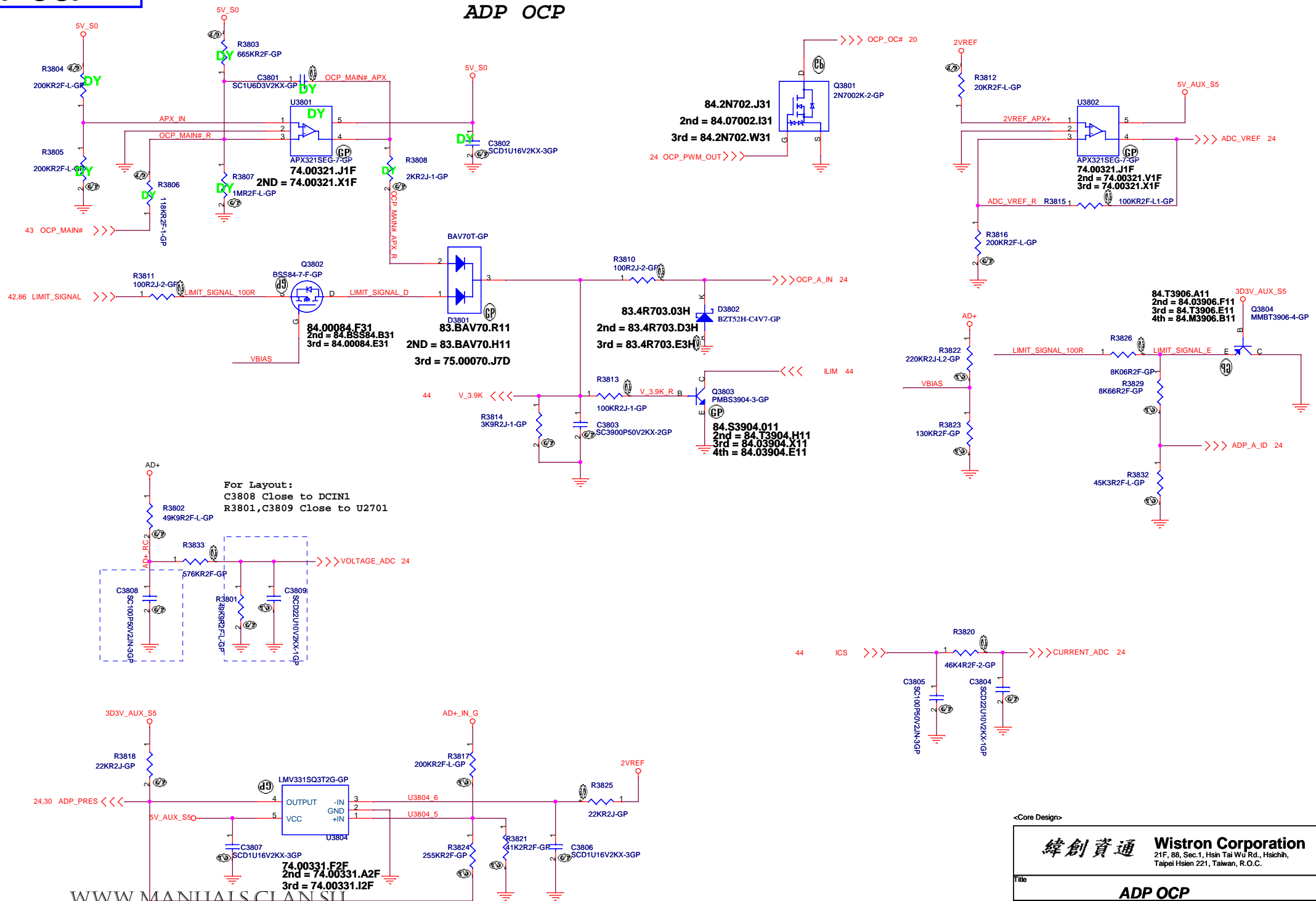
| | | |
|---------------------------------------|--|-----------------|
| Size A3 | Document Number 2013 S-Series Shark Bay 14 15 17 | Rev 1 |
| Date: Wednesday, July 03, 2013 | Sheet 35 of 103 | |

Run Power

+5VALW to +5VS Transfer
 +3VALW to +3VS Transfer
 +1.5VU to +1.5VS Transfer
 +V1.05M_LAN to +V1.05S Transfer



ADP OCP





<Core Design>

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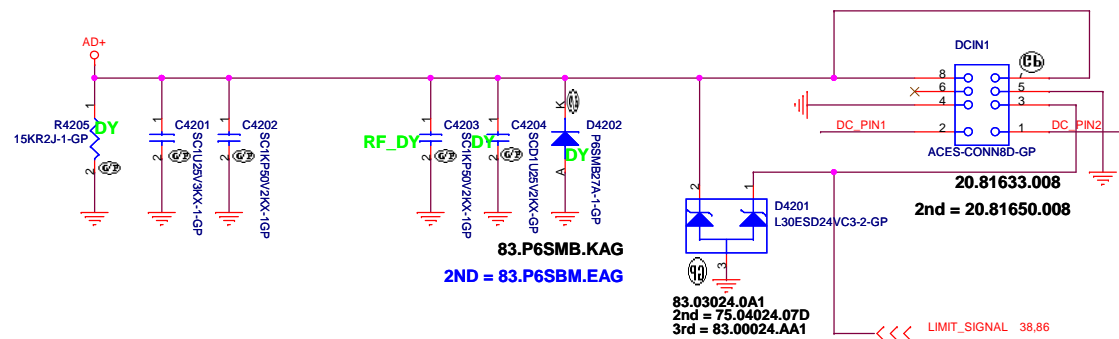
Title

1D05 M

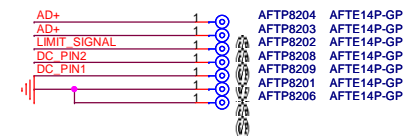
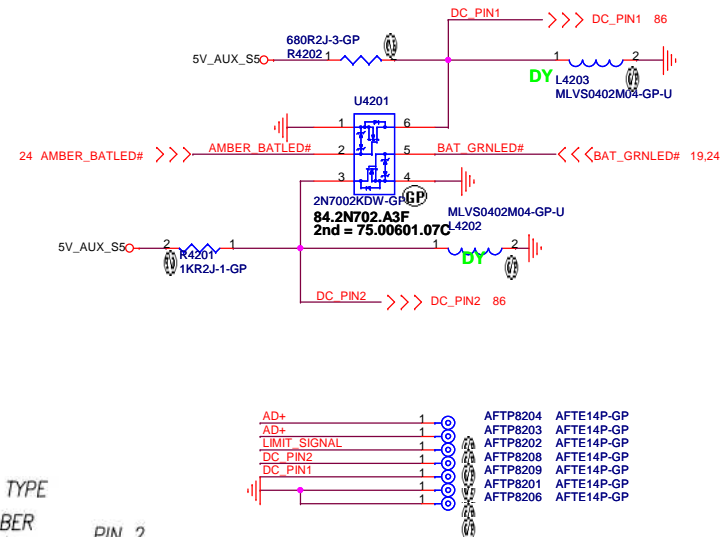
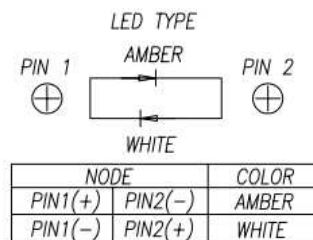
| | | |
|--------------------------------|----------------------------------|-----|
| Size | Document Number | Rev |
| A3 | 2013 S-Series Shark Bay 14 15 17 | 1 |
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| | | |
|--------------------------------|----------------------------------|-----|
| <Variant Name> | | |
| Title | | |
| <Title> | | |
| Size | Document Number | Rev |
| A2 | 2013 S-Series Shark Bay 14 15 17 | 1 |
| Date: Wednesday, July 03, 2013 | | |
| Sheet 40 of 103 | | |

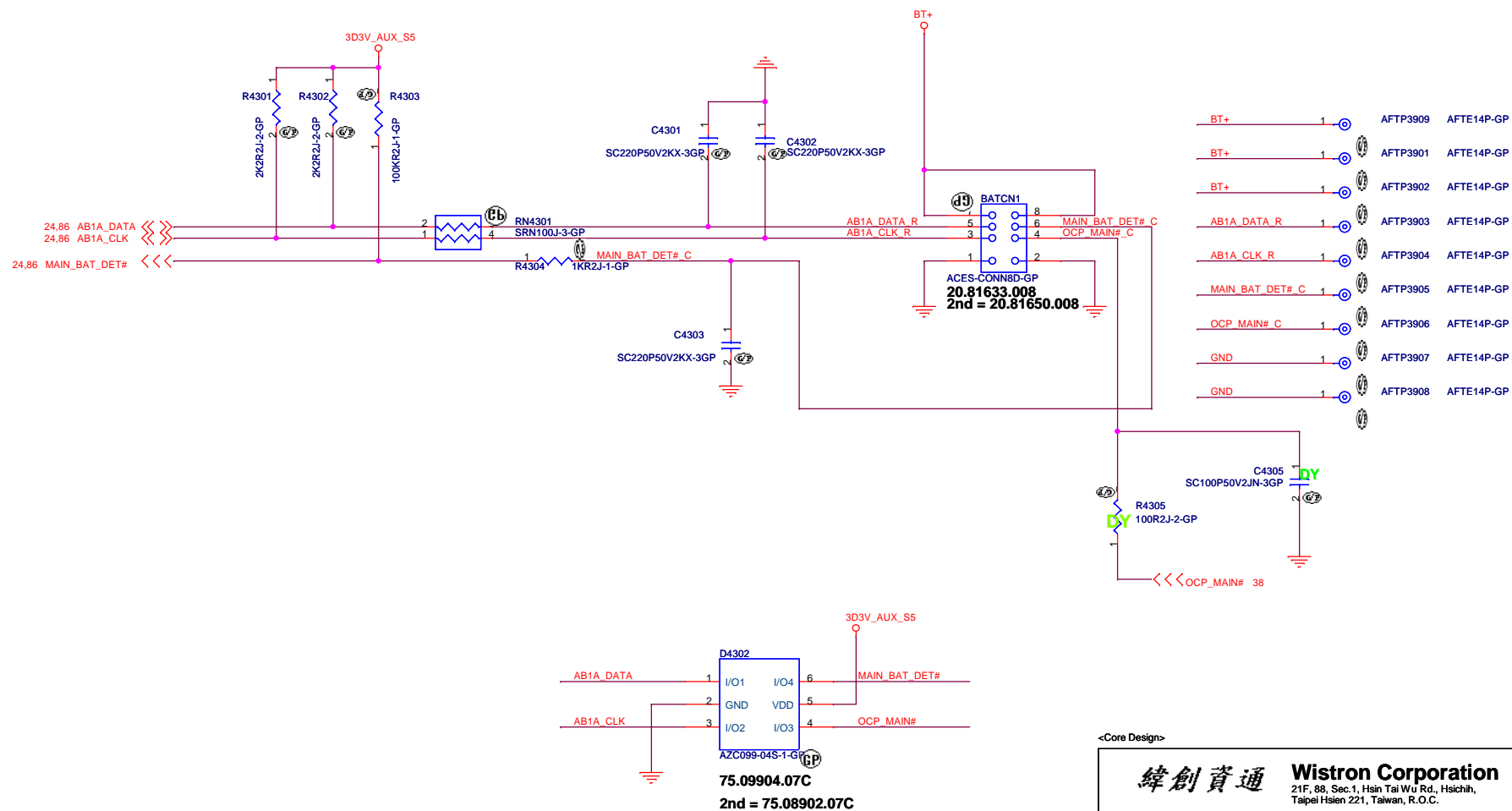
Adaptor in to generate DCBATOUT



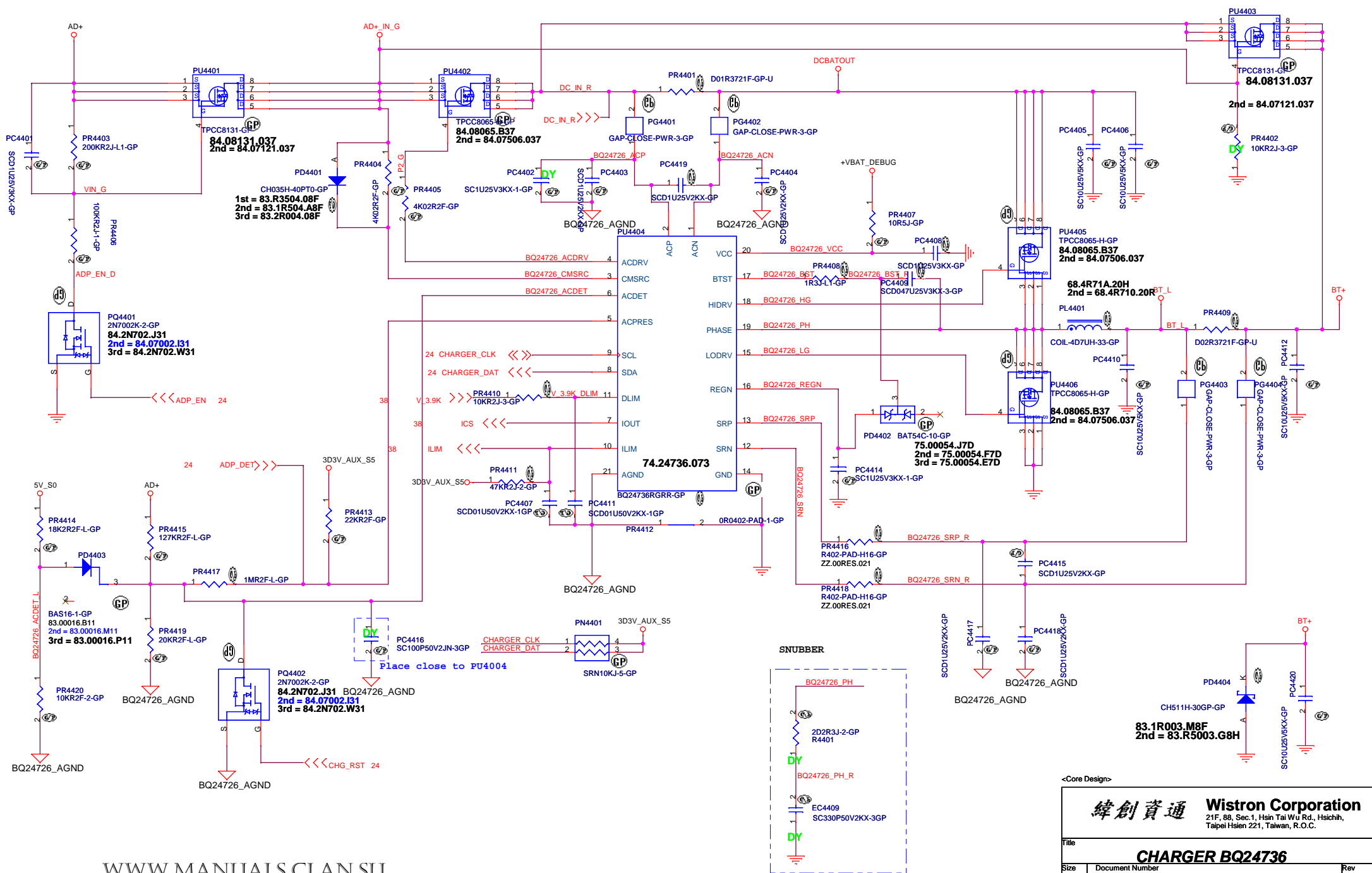
| | KBC pin 120 BAT_GRPLED# | KBC pin 113 AMBER_BATLED# |
|---------|----------------------------|------------------------------|
| Amber | High | Low |
| White | Low | High |
| LED OFF | Low | Low |

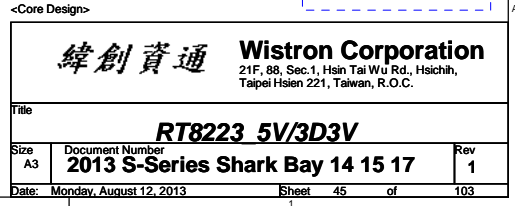


Battery Connector

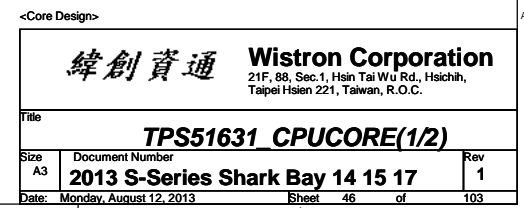


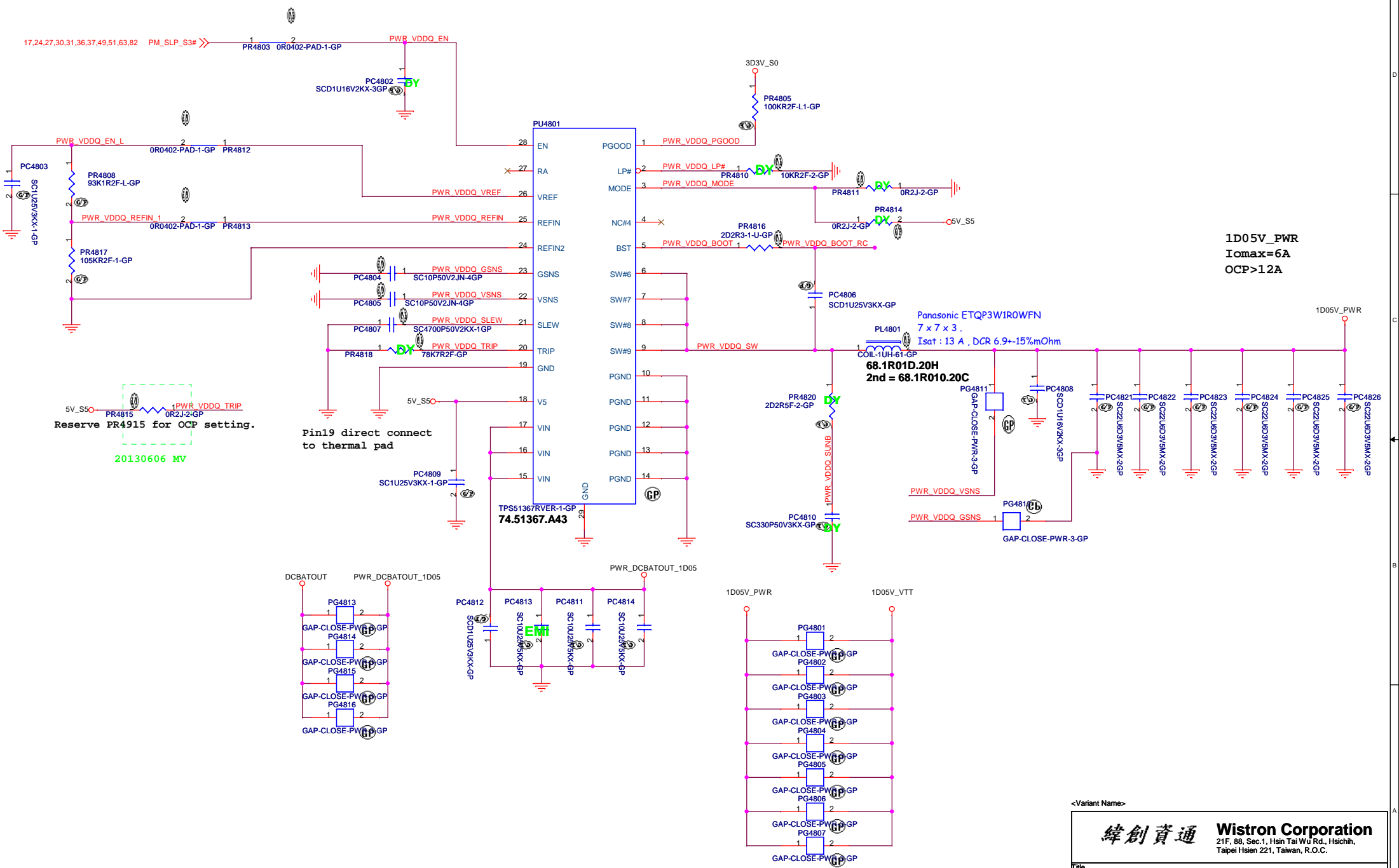
BQ24736 for CHARGER





47W:
PR4611 90.9K(64.90925.6DL)
PR4615 274K(64.27435.6DL)
PR4614 226K(64.22635.6DL)





1D05V_PWR
I_{omax}=6A
OCP>12A

Reserve PR4915 for OCP setting.
20130606 MV

Pin19 direct connect
to thermal pad

TPS51367RVER-1-GP
74.51367.A43

Panasonic ETQP3W1R0WFN
7 x 7 x 3 .
Isat : 13 A , DCR 6.9+-15% mOhm
68.1R01D.20H
2nd = 68.1R010.20C

<Variant Name>

| | | |
|--|-----------------|-----------------|
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| Title TPS51367 1D05V VTT | | |
| Size A3 | Document Number | Rev 1 |
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(Blanking)

<Core Design>

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Title

(Reserved)

Size
A3

Document Number

Rev

2013 S-Series Shark Bay 14115 17

Date: Wednesday, July 03, 2013

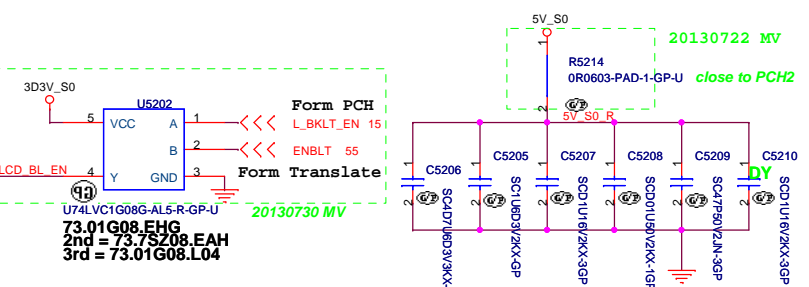
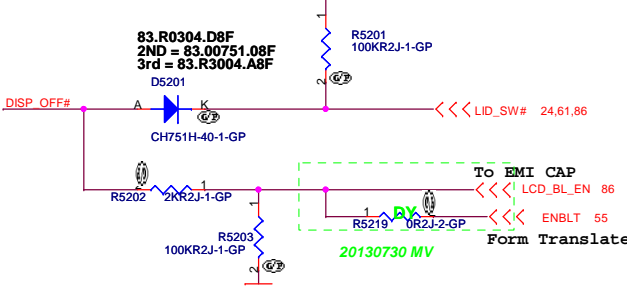
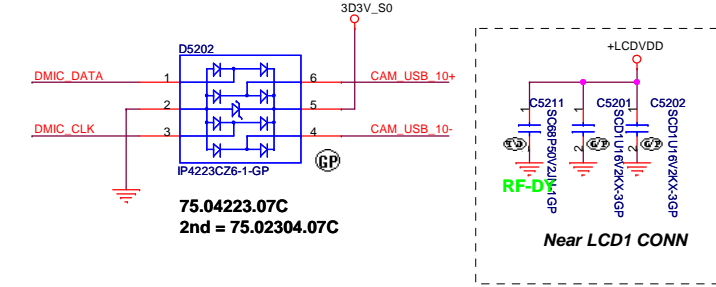
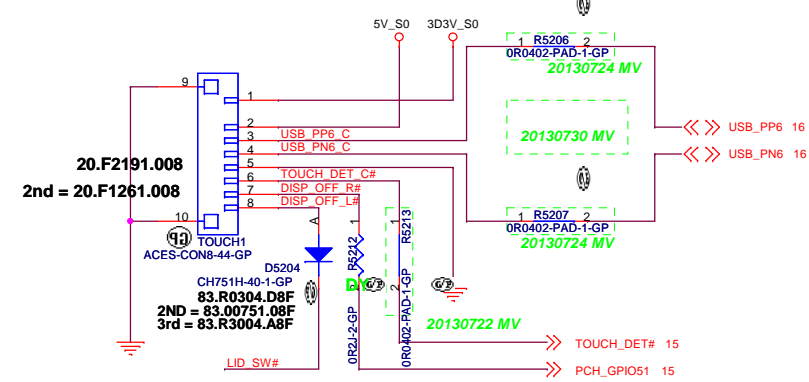
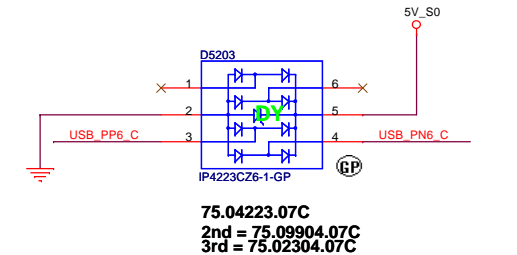
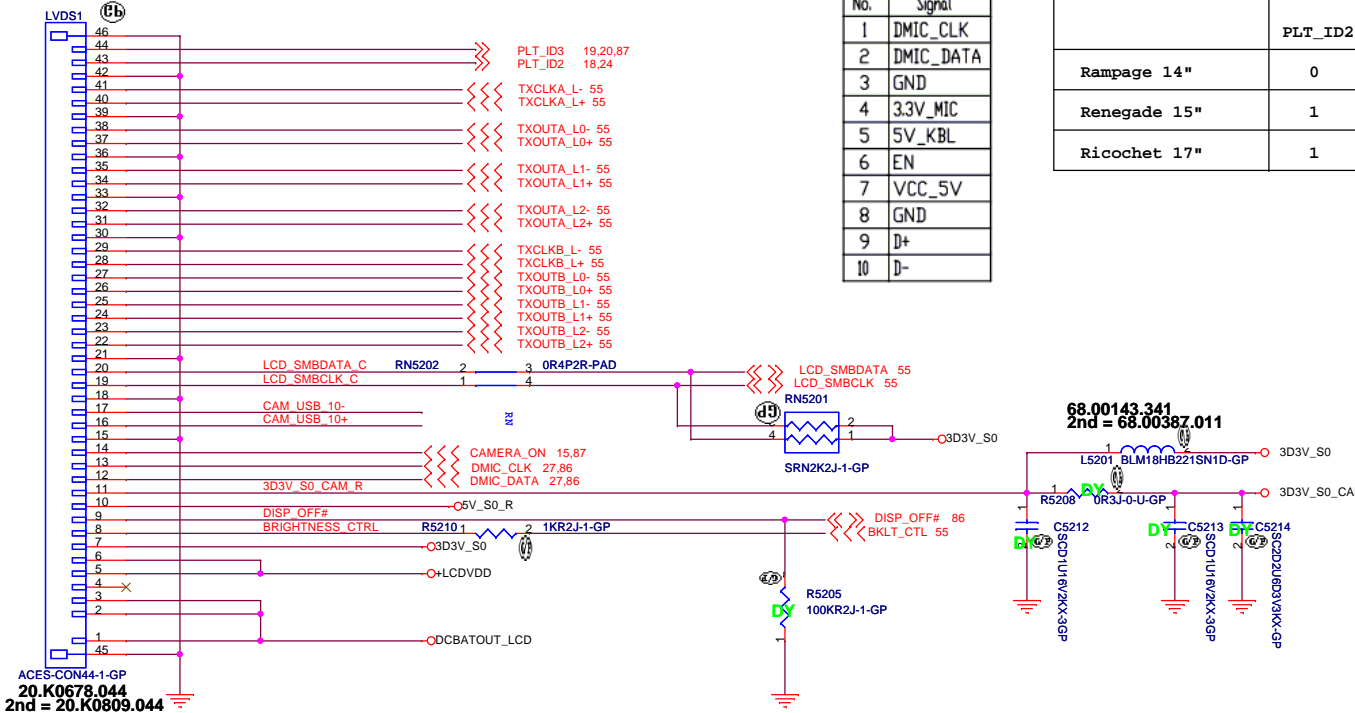
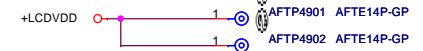
Sheet 50 of 103

LCD Connector

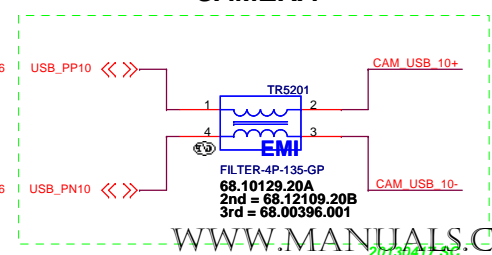
Camera Pin Define

| No. | Signal |
|-----|-----------|
| 1 | DMIC_CLK |
| 2 | DMIC_DATA |
| 3 | GND |
| 4 | 3.3V_MIC |
| 5 | 5V_KBL |
| 6 | EN |
| 7 | VCC_5V |
| 8 | GND |
| 9 | D+ |
| 10 | D- |

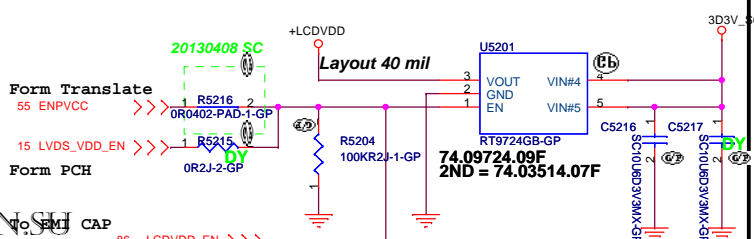
| | GPIO23 | GPIO69 |
|--------------|---------|---------|
| Rampage 14" | PLT_ID2 | PLT_ID3 |
| Renegade 15" | 0 | 1 |
| Ricochet 17" | 1 | 1 |



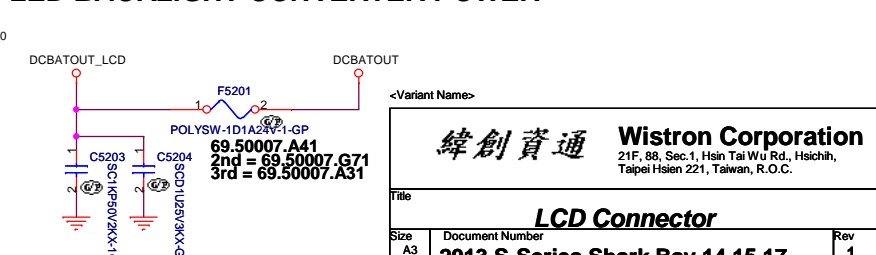
CAMERA



LCD POWER CIRCUIT



LED BACKLIGHT CONVERTER POWER

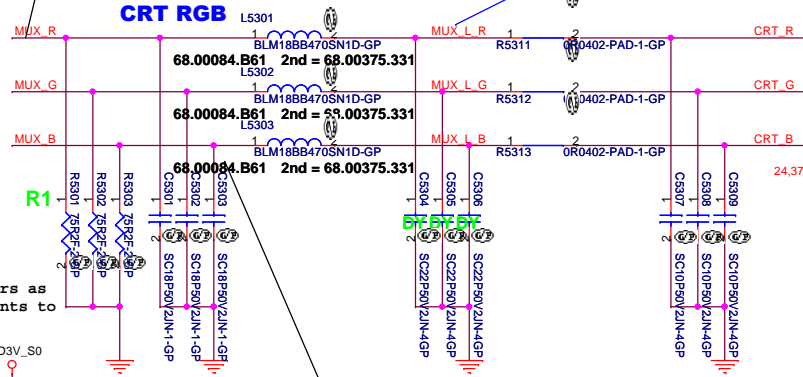


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CRT Connector

CRT1
Transmission line
characteristic
impedance for RGB
signals $Z_0 = 37.5 \text{ Ohm}$

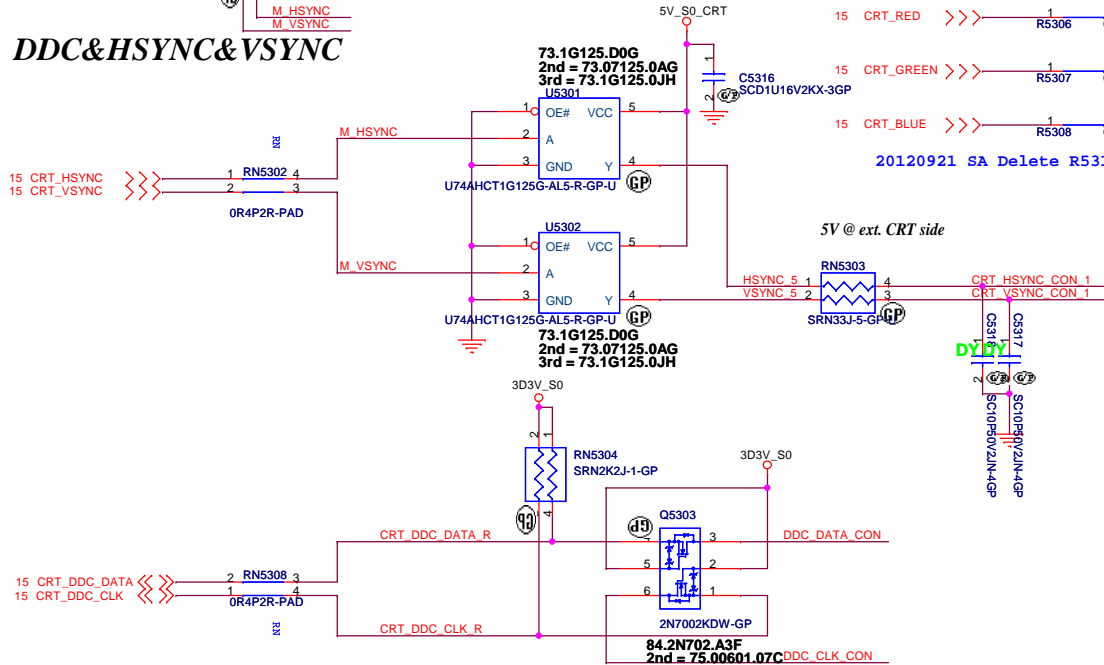
Transmission line characteristic
impedance $Z_0 = 50 \text{ Ohm}$



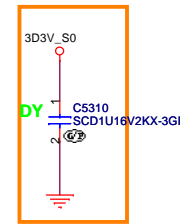
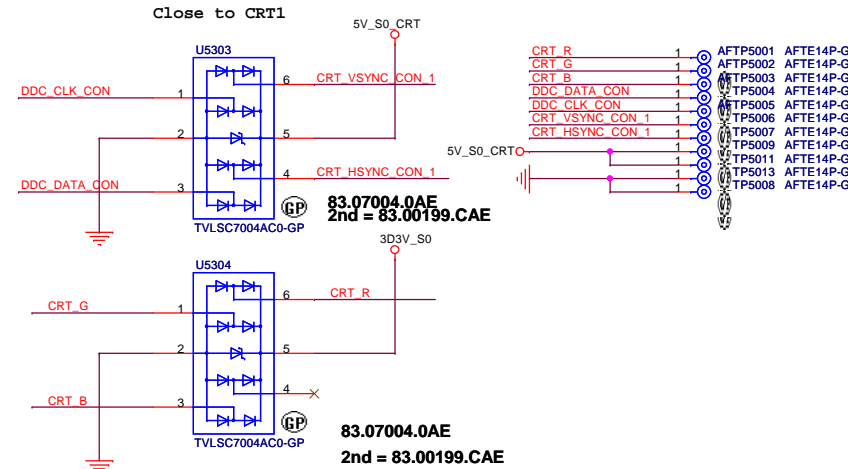
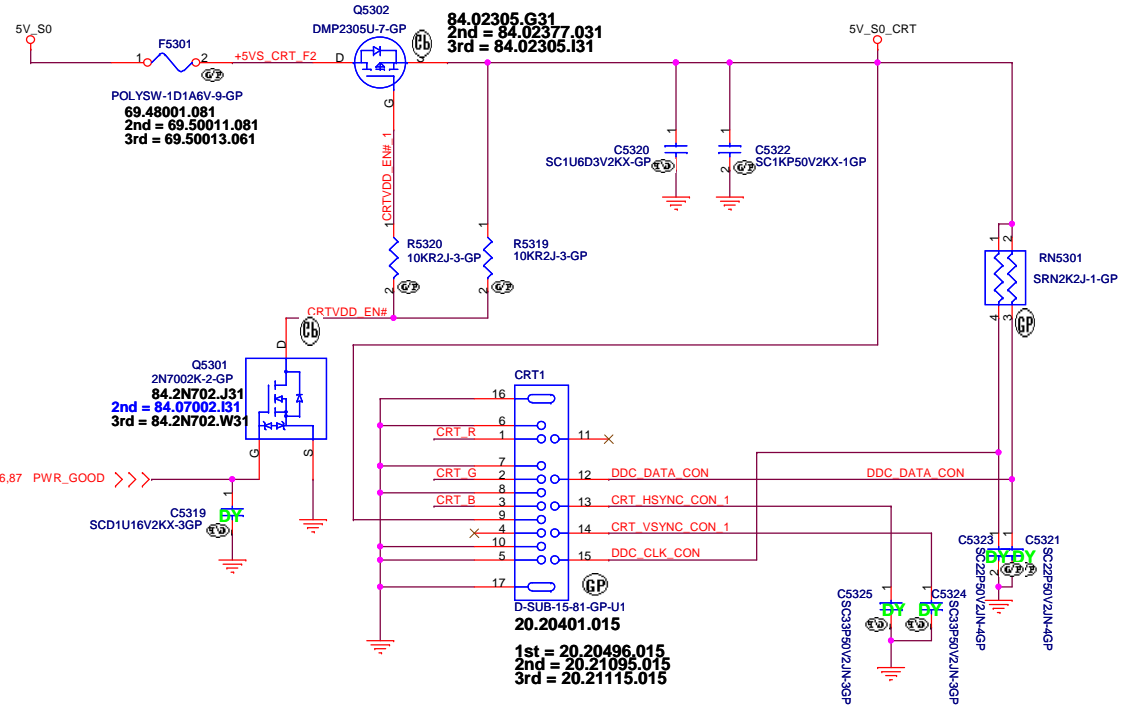
Place these resistors as
the closest components to
connector CRT1

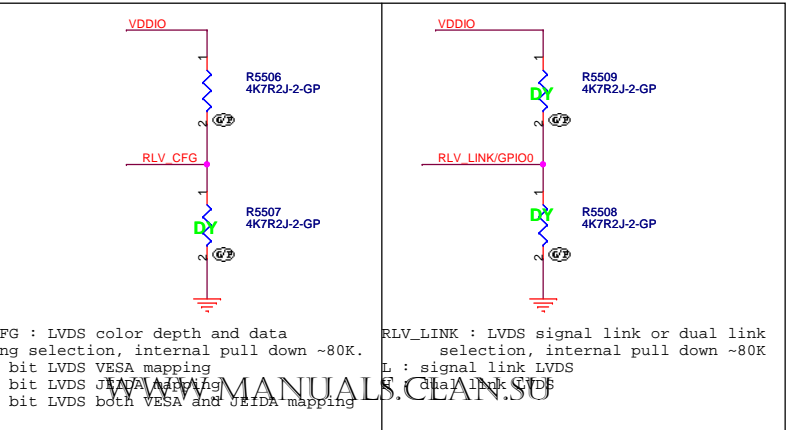
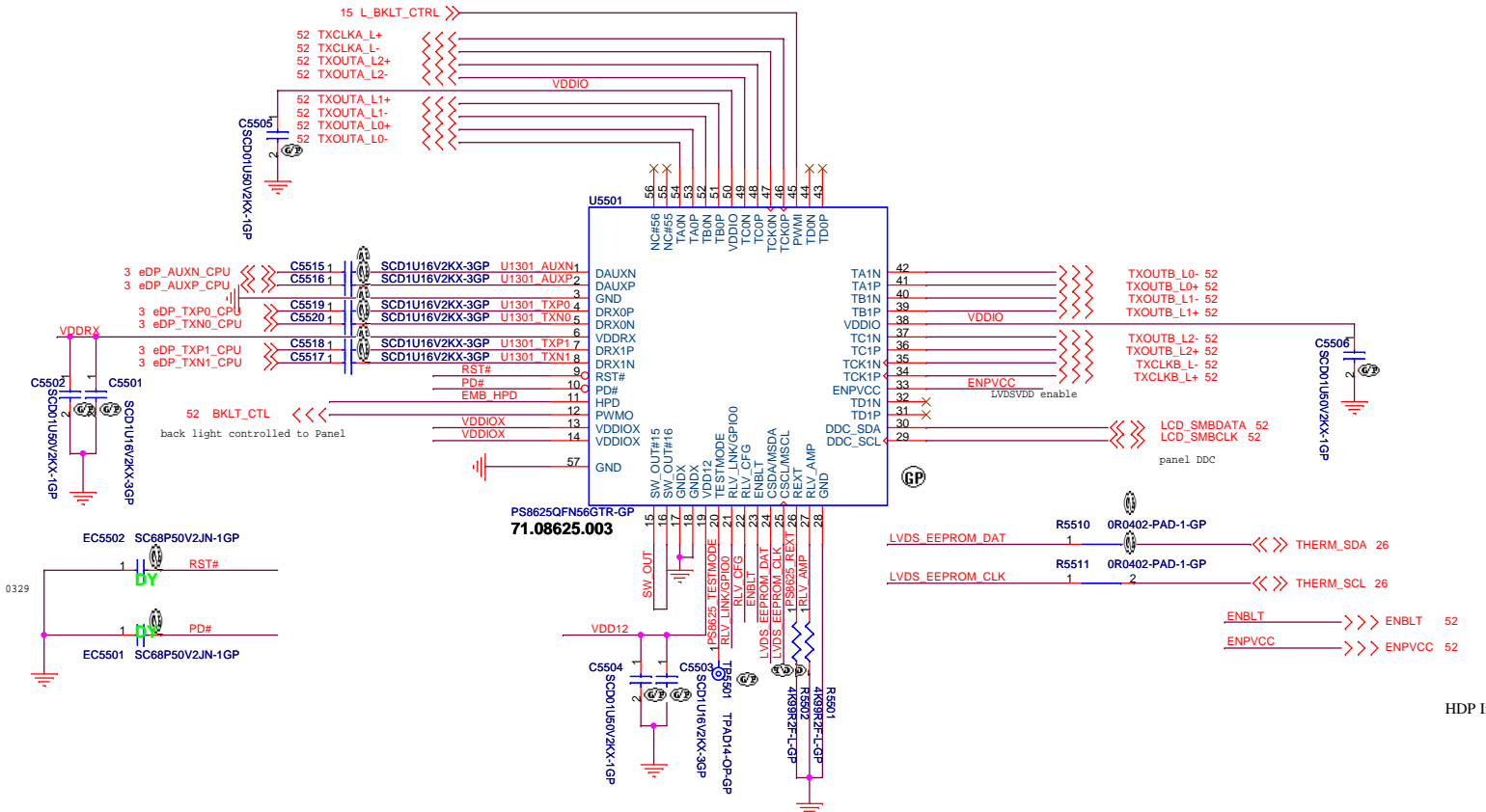
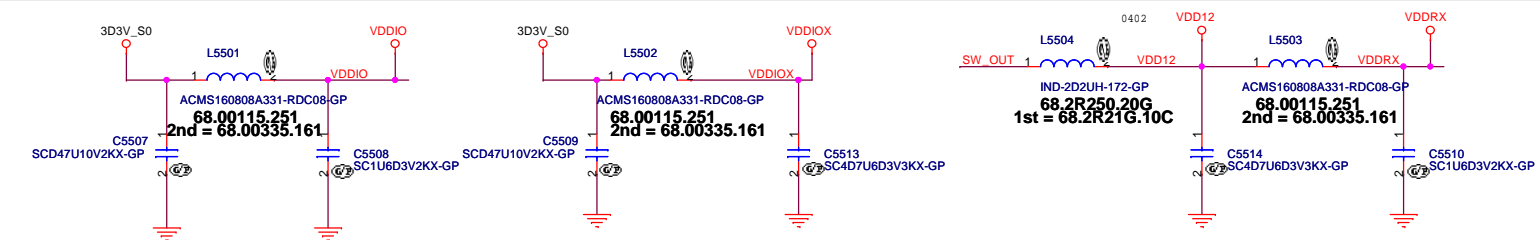
Transmission line characteristic
impedance $Z_0 = 50 \text{ Ohm}$

DDC&HSYNC&VSYNC



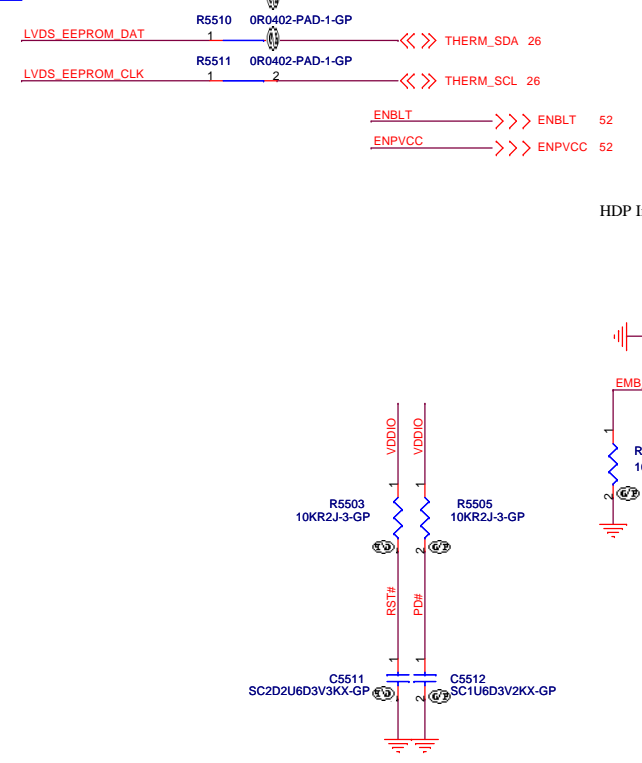
WWW.MANUALS.CLAN.SU



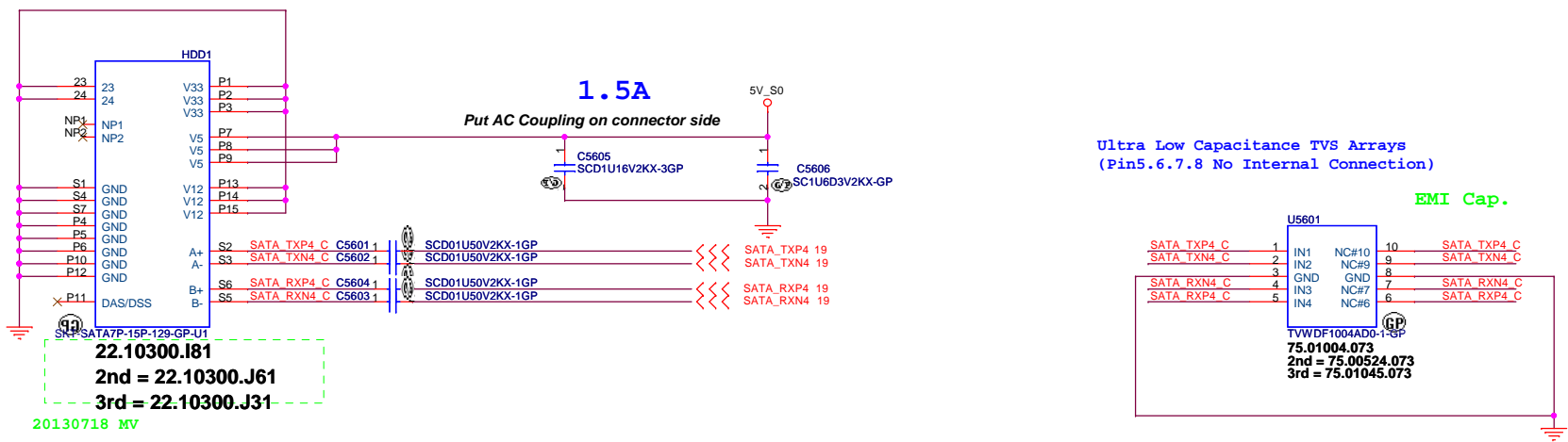


RLV_CFG : LVDS color depth and data mapping selection, internal pull down ~80K.
L : 8 bit LVDS VESA mapping
M : 8 bit LVDS JEIDA mapping
H : 6 bit LVDS both VESA and JEIDA mapping

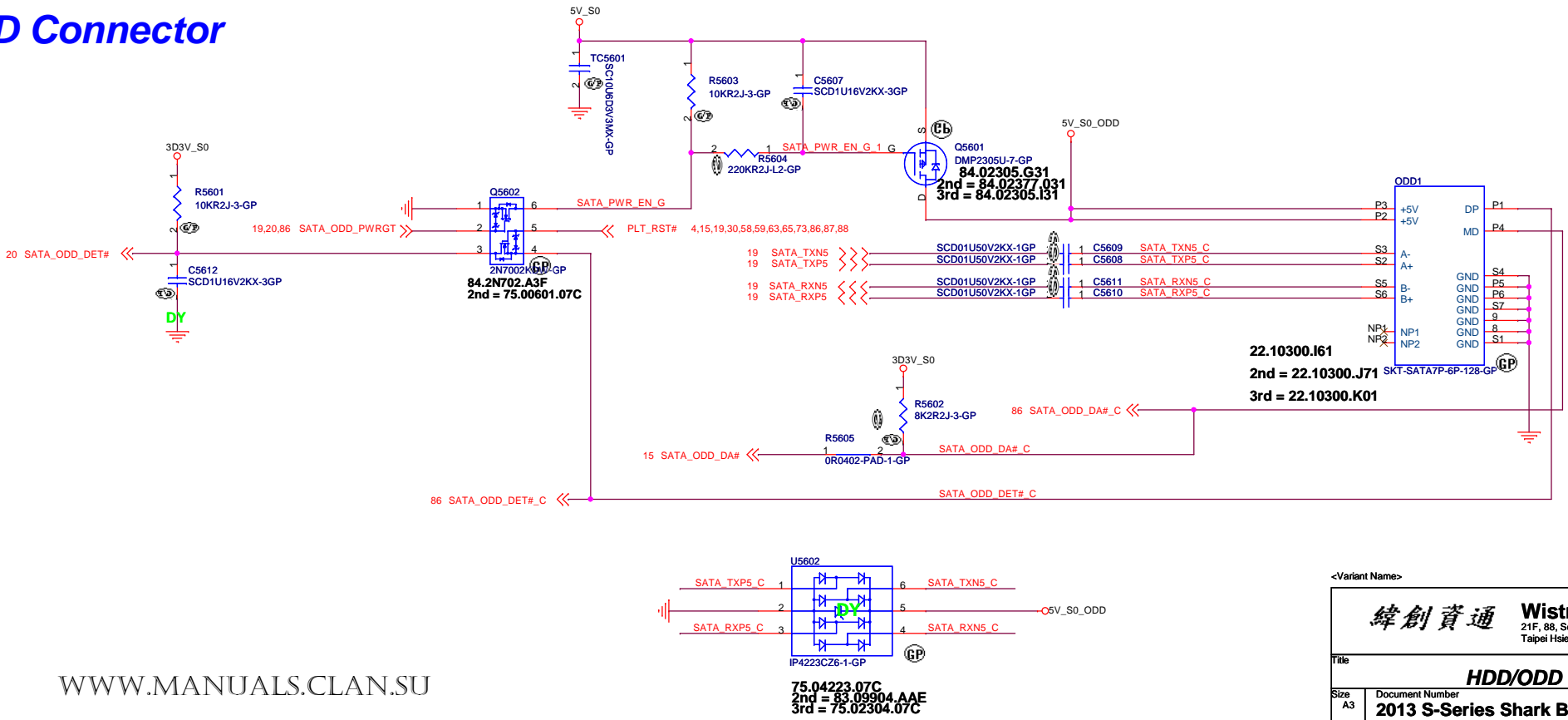
RLV_LINK : LVDS signal link or dual link selection, internal pull down ~80K
L : signal link LVDS
M : dual link LVDS
H : dual link LVDS



HDD Connector



ODD Connector



(Blanking)

<Core Design>

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Title

(Reserved)

Size
A3

Document Number

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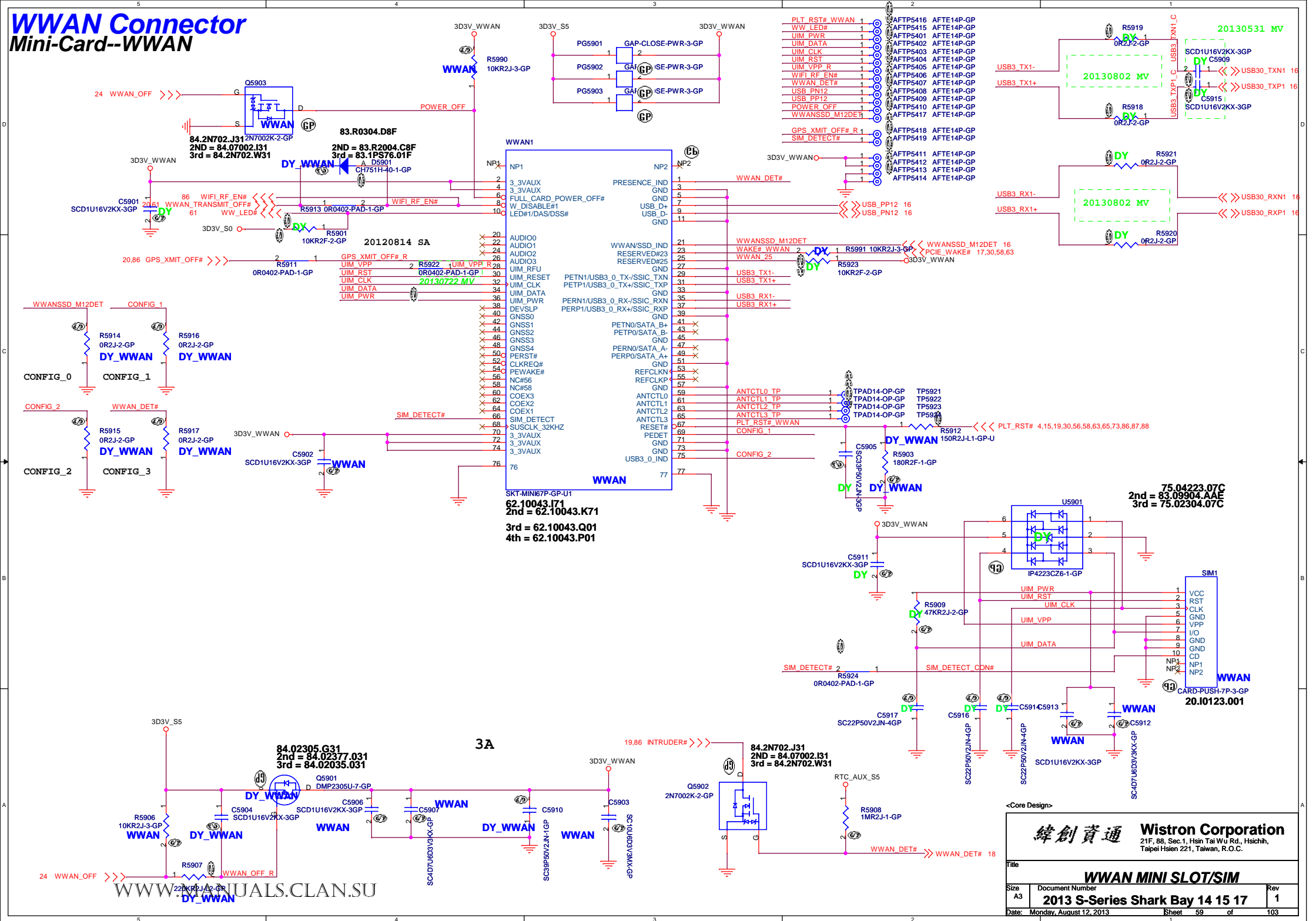
1

Mini-Card--WLAN (Half)



WWAN Connector

Mini-Card--WWAN





<Variant Name>

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Title

Flash

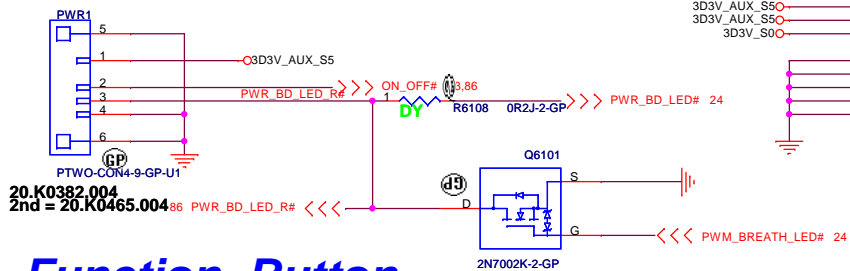
Size
A3

Document Number
2013 S-Series Shark Bay 14 15 17

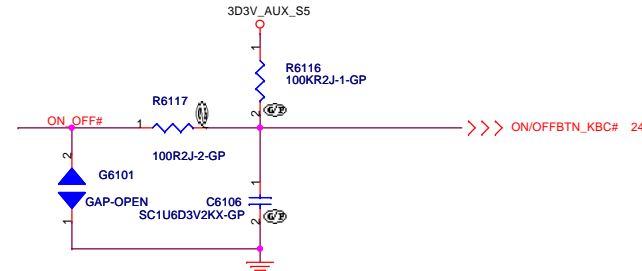
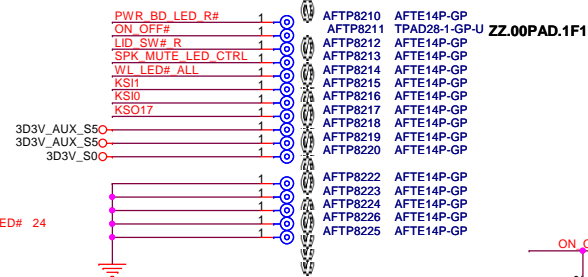
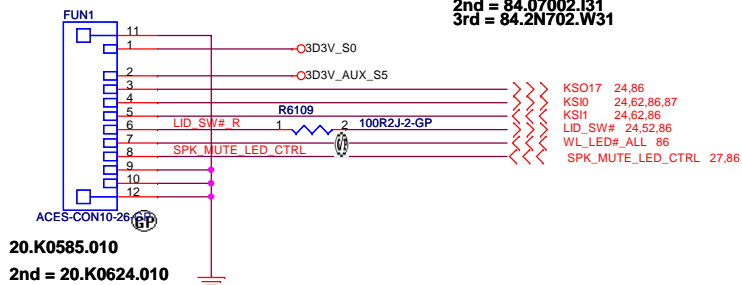
Rev
1

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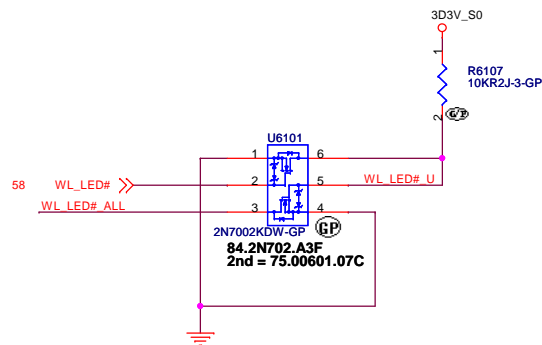
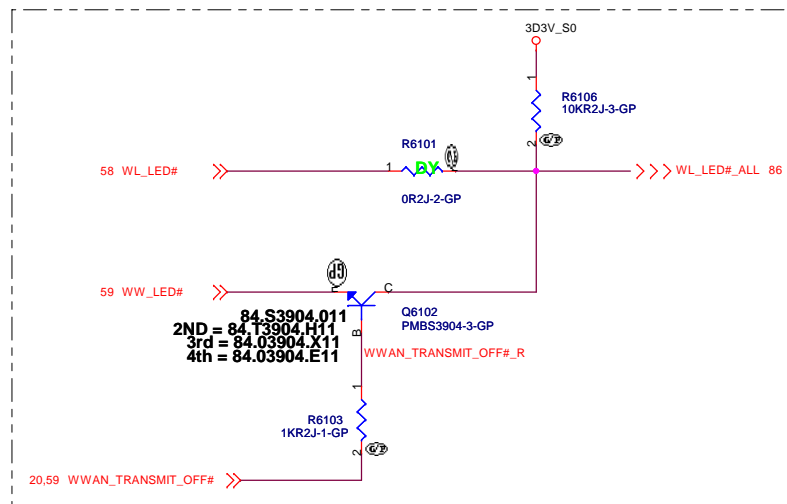
Power Button



Function Button

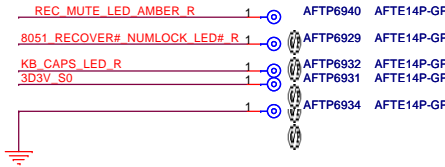
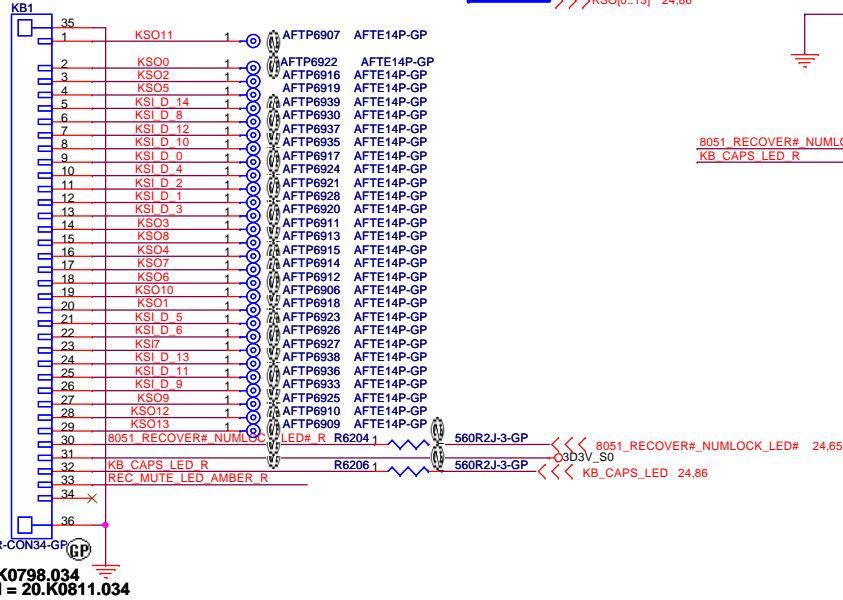


WLAN / WWAN POWER LED

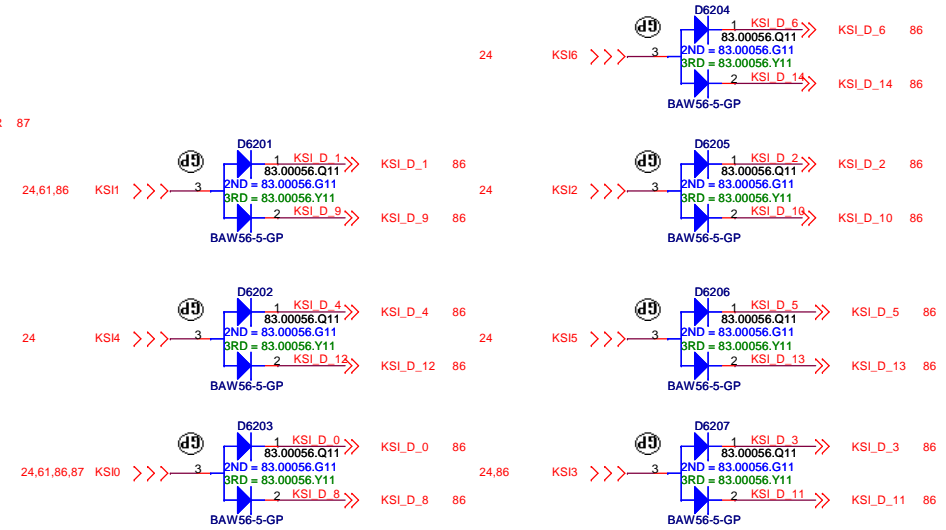
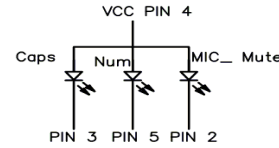


Keyboard Connector

<<< KSI[0..7] 24,61,86,87
>>> KSO[0..13] 24,86

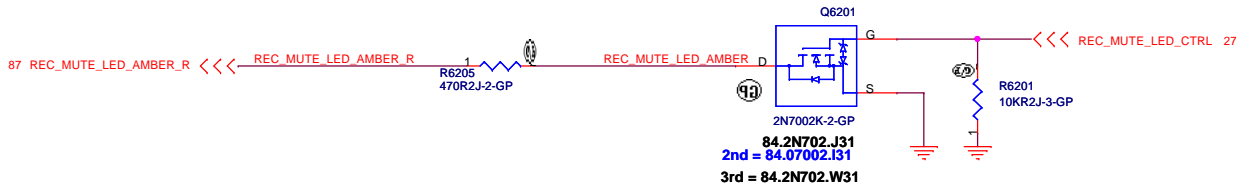


8051_RECOVER#_NUMLOCK_LED#_R >>> 8051_RECOVER#_NUMLOCK_LED#_R 87
KB_CAPS_LED_R >>> KB_CAPS_LED_R 87



On Keyboard LEDs

<MUTE> Internal MIC ON= No light; OFF/Mute= Amber



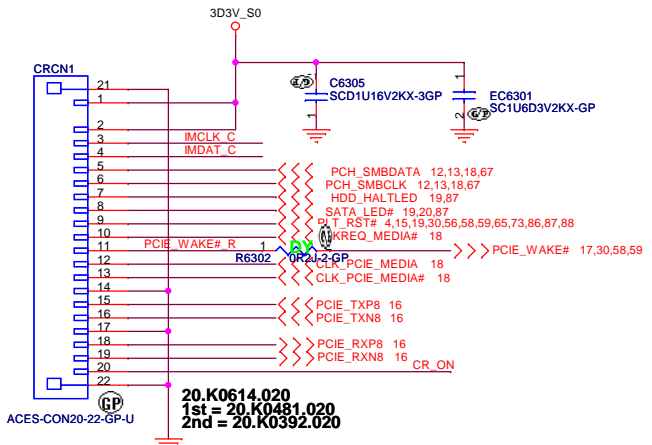
<Core Design>

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| Title | | |
|----------------------------------|-----------------|--------|
| Key Board/Touch Pad | | |
| Size A3 | Document Number | Rev 1 |
| 2013 S-Series Shark Bay 14 15 17 | | |
| Date: Monday, August 12, 2013 | Sheet 62 | of 103 |

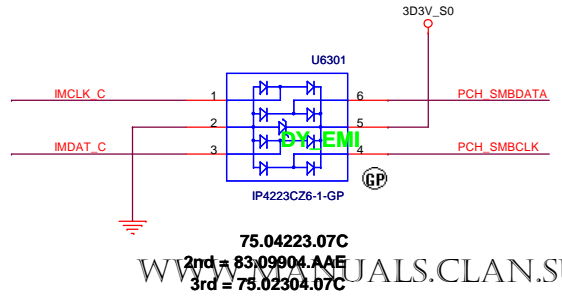
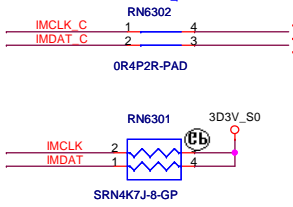
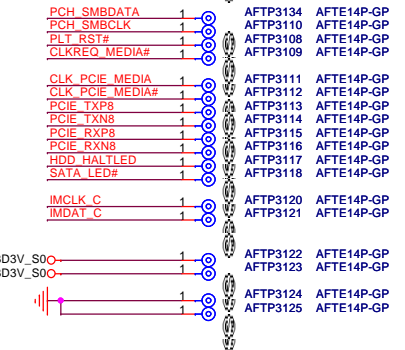
Audio Board +Touch Pad + Card Reader IC Connector

Right Side Audio & FP & USB Connector



PCIE_WAKE# 1 AFTP3127 AFTE14P-GP
CR_ON 1 AFTP3126 AFTE14P-GP

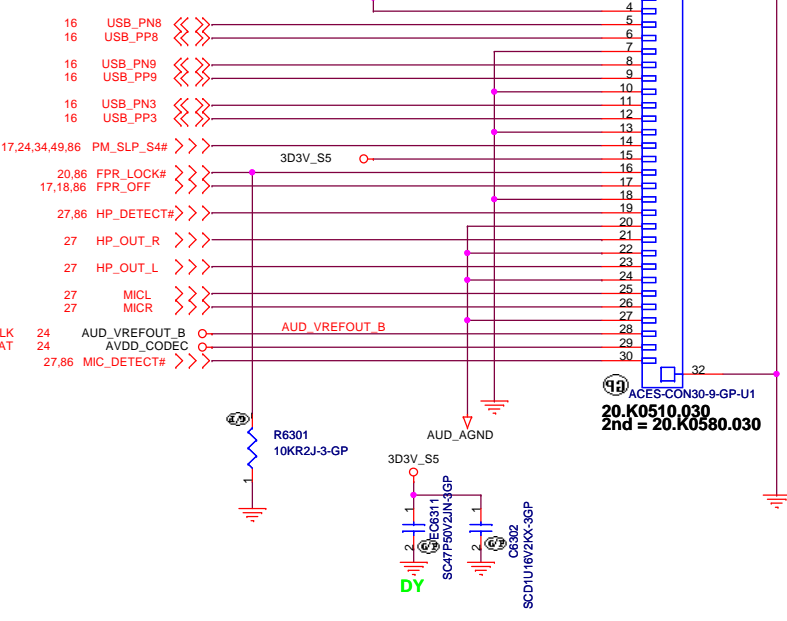
Fiji and Python no this function
Please connect to pin 11 pin20



Pinout on customer's board, as in the PDG, CDI #486713,

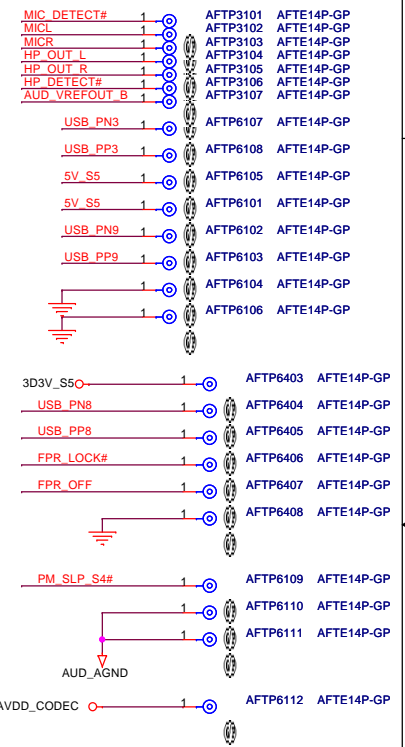
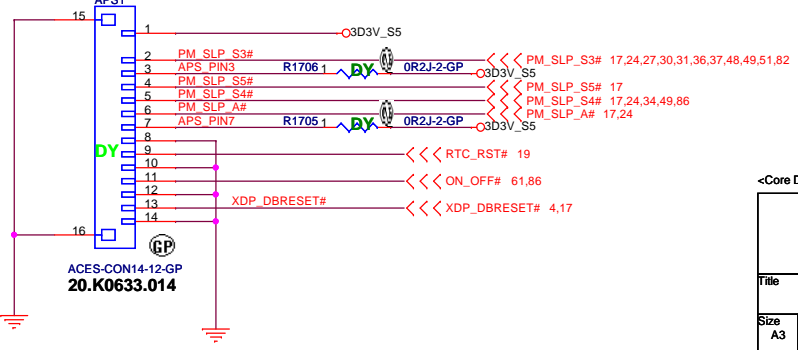
| Pin | Signal Name |
|-----|-------------|
| 1 | VccSus3_3 |
| 2 | SLP_S3# |
| 3 | VccDSW3_3 |
| 4 | SLP_S5# |
| 5 | SLP_S4# |
| 6 | SLP_A# |
| 7 | +V3,3DS |
| 8 | GND |
| 9 | RTCRST# |
| 10 | GND |
| 11 | PWRBTN# |
| 12 | GND |
| 13 | SYS_RESET# |
| 14 | GND |

20120921 Delete R6303 R6304



APS1 for QT test do not install

No support DSW/Deep sleep, connect to 3D3V_S5



<Core Design>

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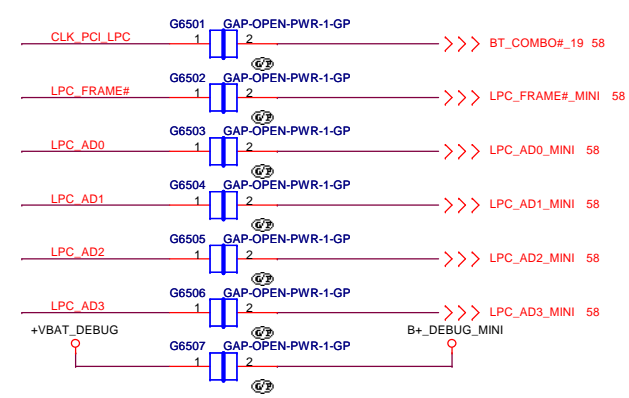
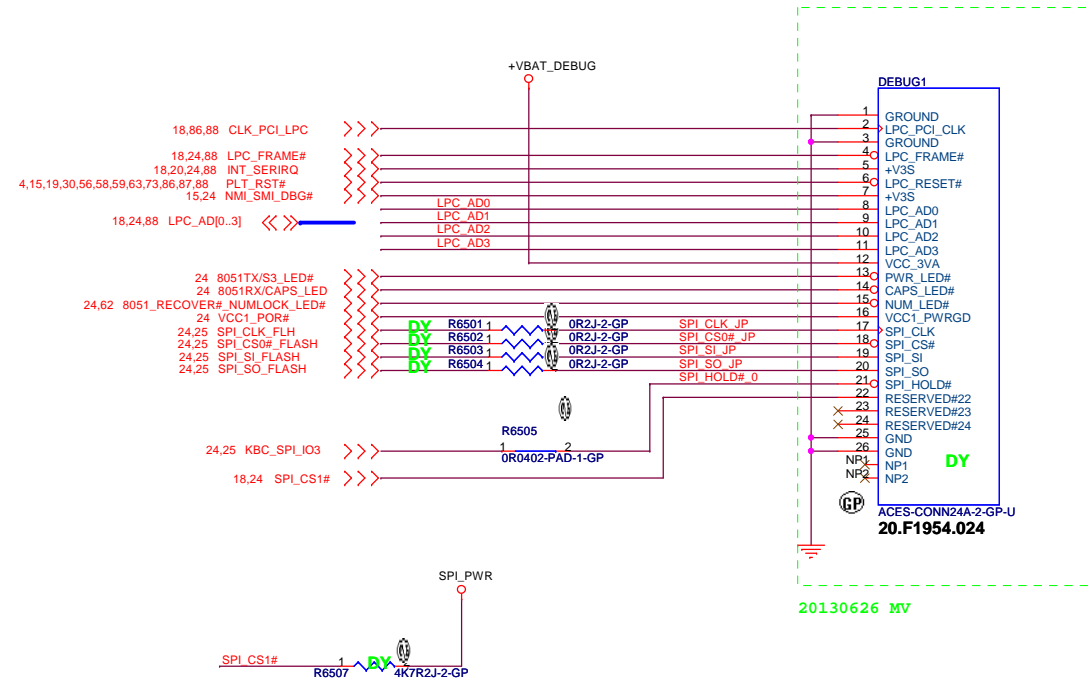
Title

IO Board Connector

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24 PIN LPC DEBUG CONN.



(Blanking)

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Title

SENSOR HUB

Size
A3

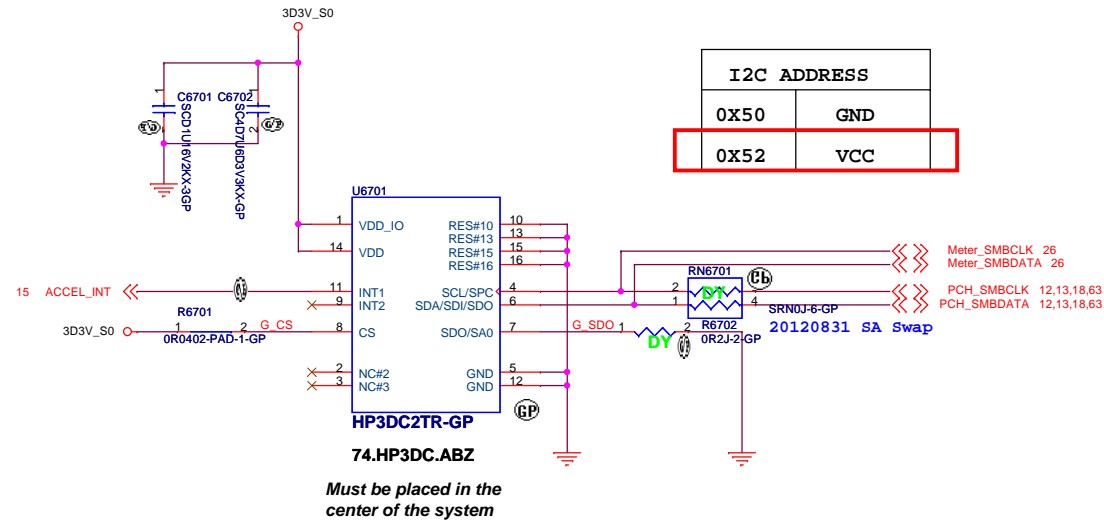
Document Number
2013 S-Series Shark Bay 14 15 17

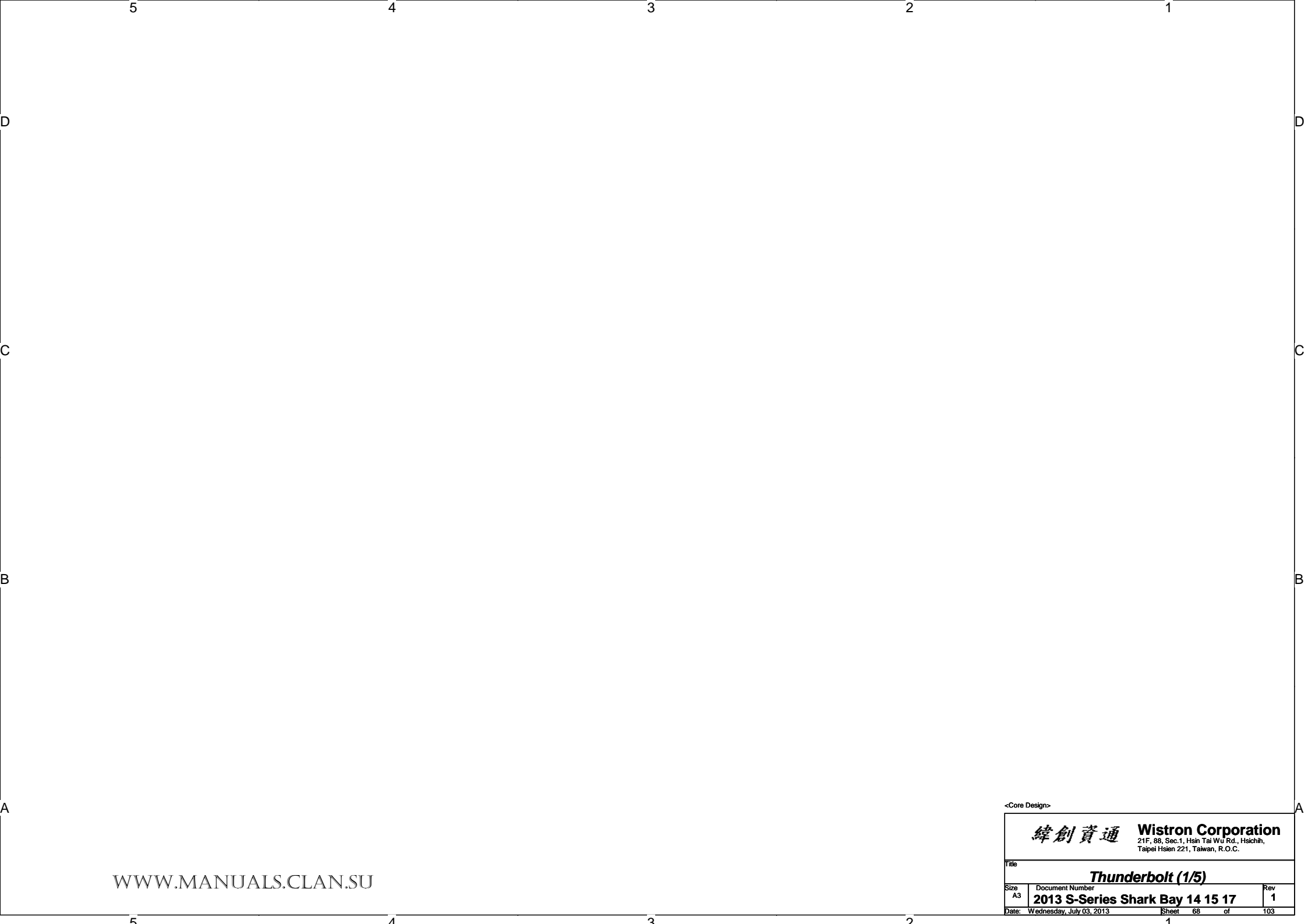
Date: Wednesday, July 03, 2013

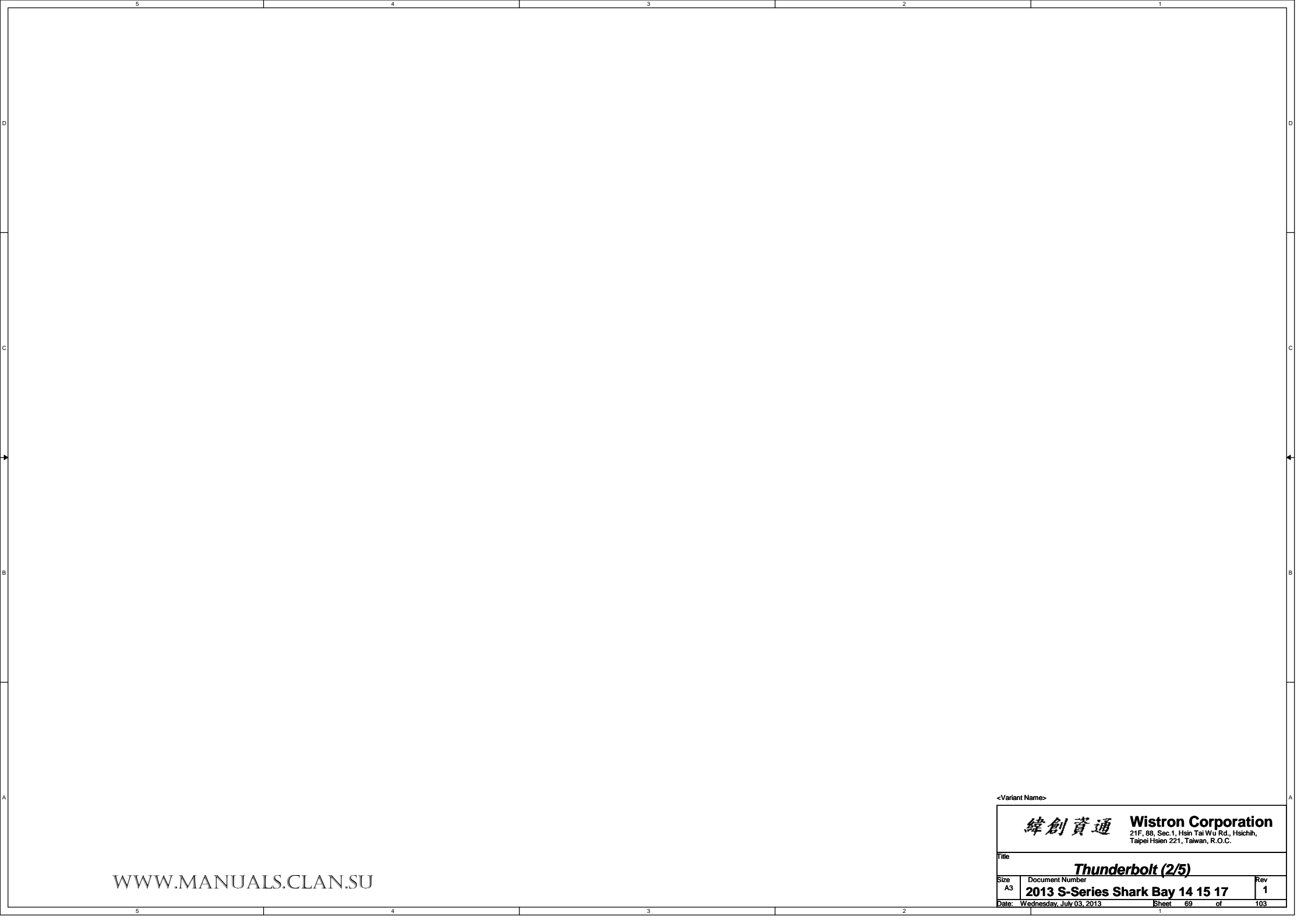
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Rev
1

ACCELEROMETER

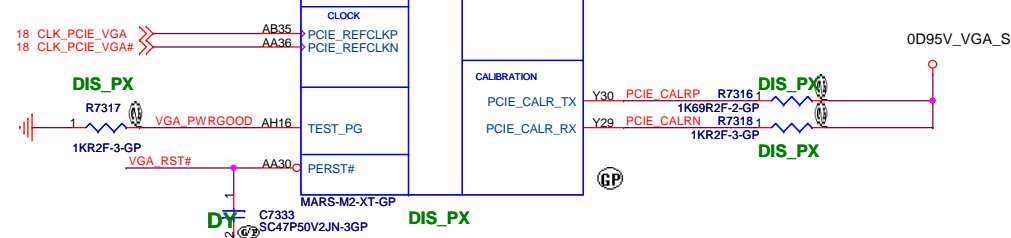
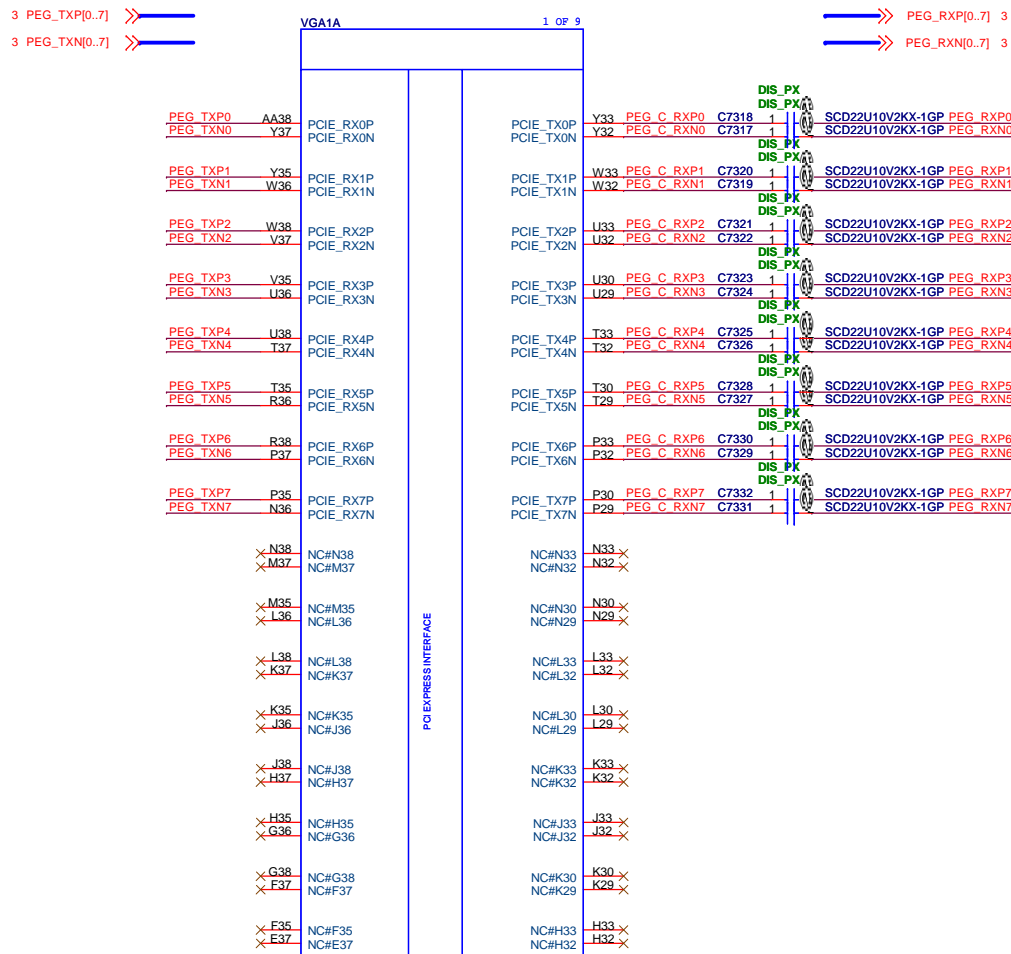






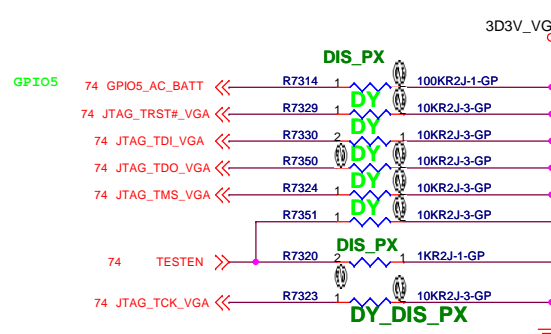
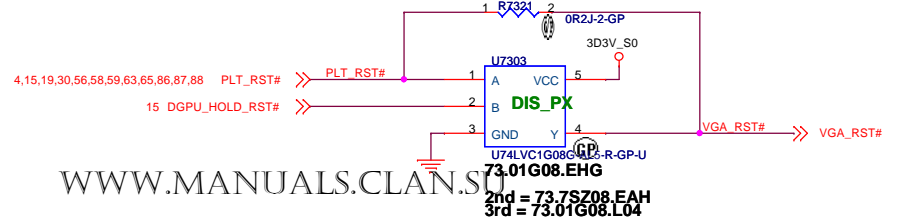
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dGPU reset for PX/SG transitions

DY_DIS_PX



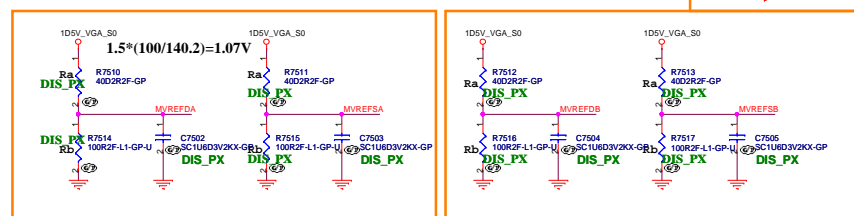
| JTAG SIGNAL OPTION | | | |
|--------------------|-------------|------------|----------------|
| Signal | Normal mode | Debug mode | pilot run mode |
| TESTEN | "1" (PU) | "1" (PU) | "0" (PD) |
| JTAG_TRST# | "0" (PD) | "1" (PU) | NC |
| JTAG_TCK | CLK | "1" (PU) | NC |
| JTAG_TMS | "1" (PU) | "1" (PU) | NC |

<Core Design>

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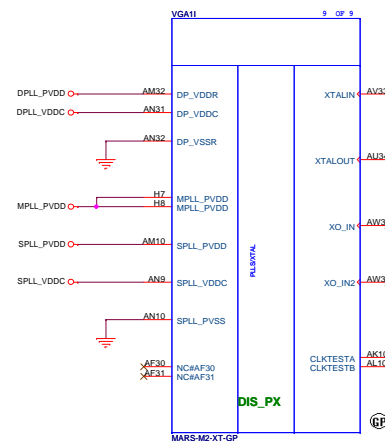
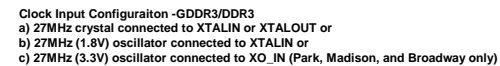
Title: **GPU (1/5) PEG**

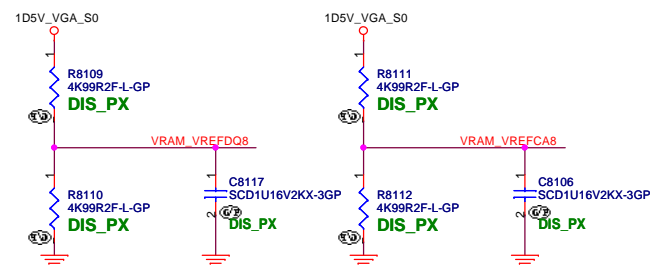
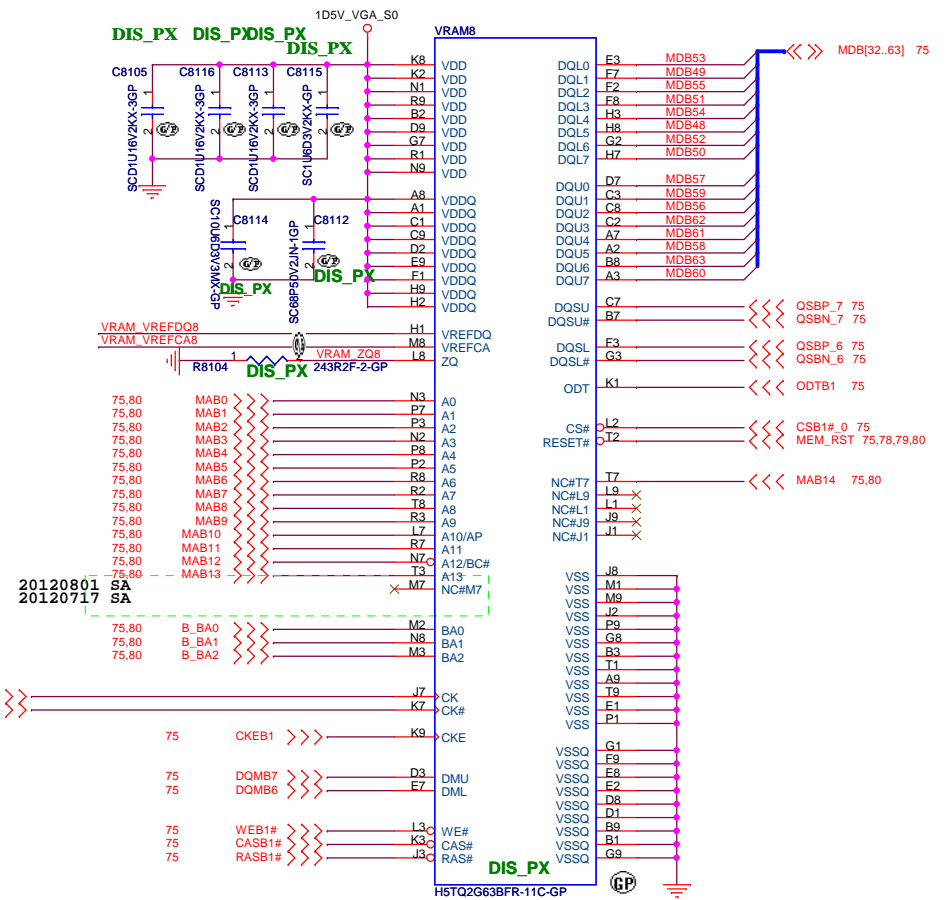
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|-------------------------------|--|-----------------|
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DDR3/GDDR3 Memory Stuff Option(Mad/Park)

WWW.MANUALS.CLAN.SU

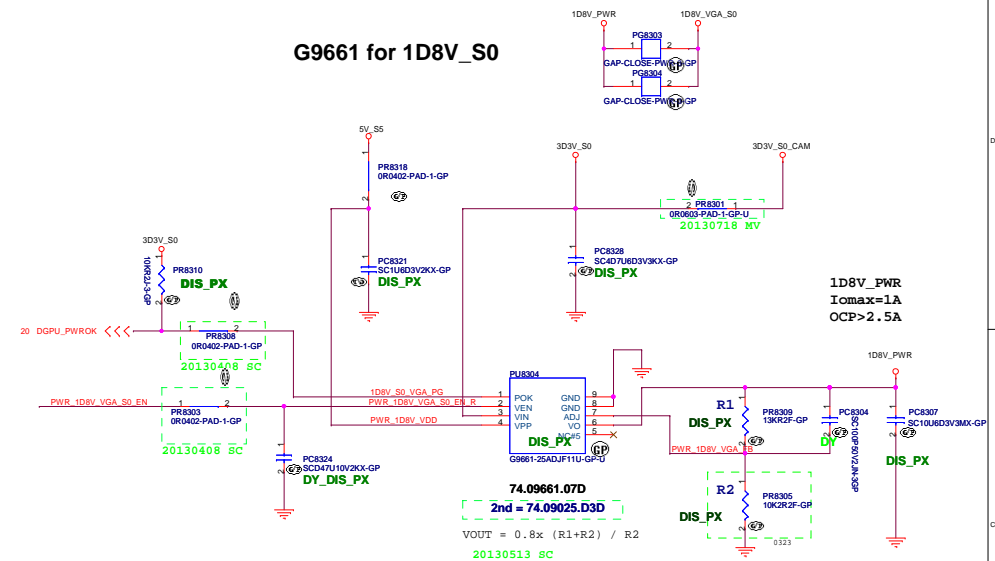




| V-BOOT | VID0 | VID1 | VID2 | VID3 | VID4 | VID5 | VID6 |
|--------|------|------|------|------|------|------|------|
| 0.85V | 0 | 0 | 1 | 0 | 1 | 1 | 0 |



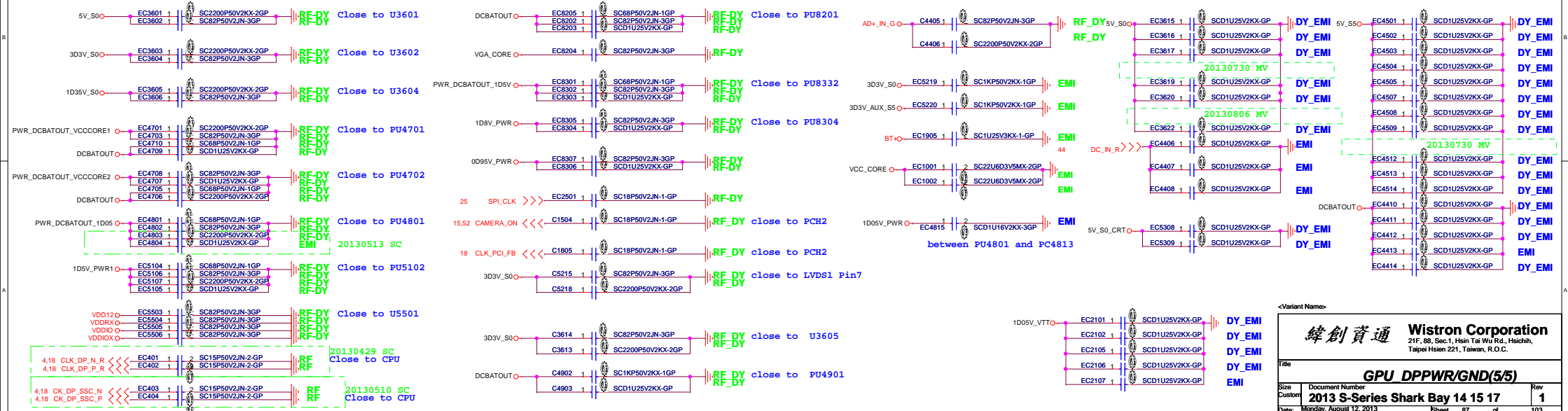
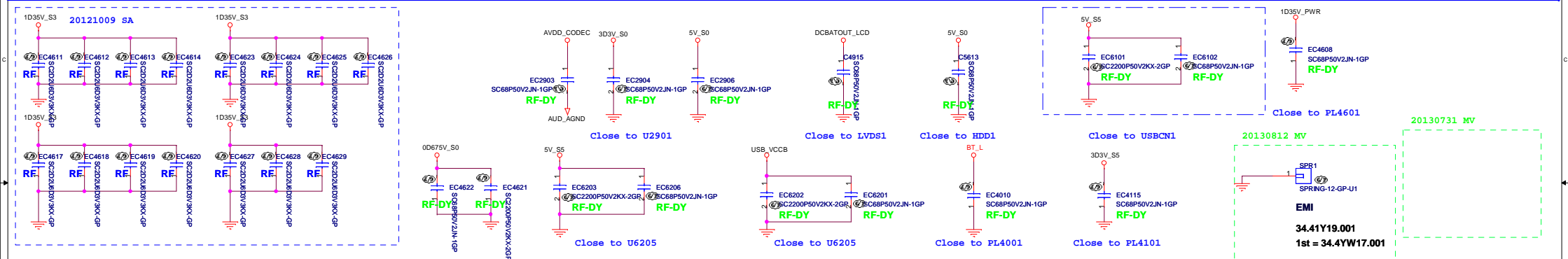
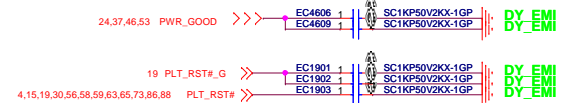
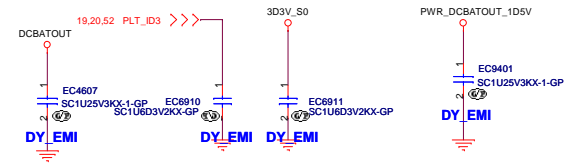
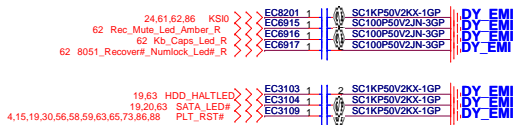
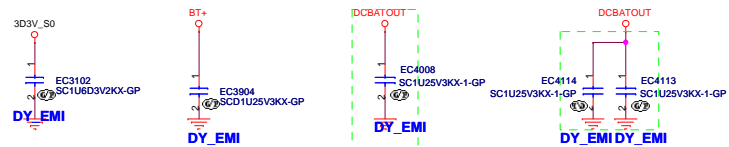
G9661 for 1D8V_S0

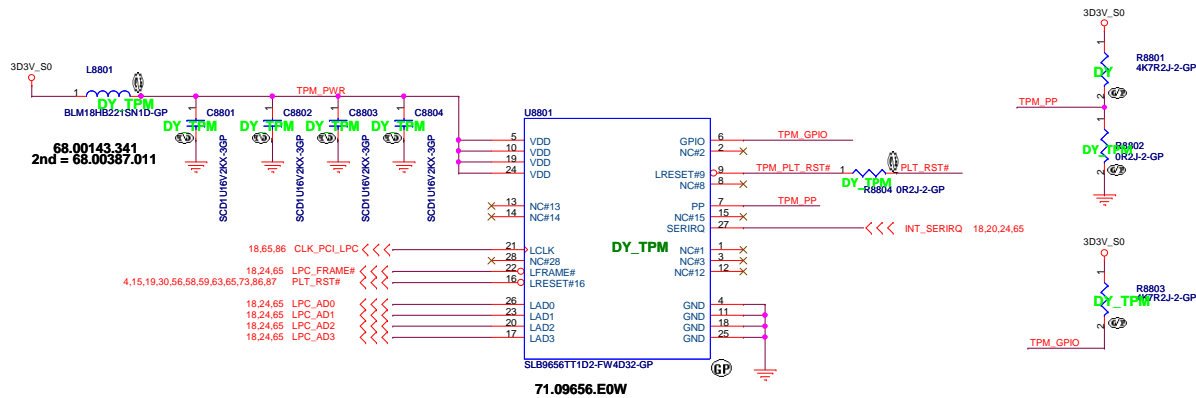
[illegible]

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| | | | |
|----------------|---|--|-----------|
| *Variant Name: | |  Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | DISCRETE VGA POWER | |
| Size A2 | Document Number | | Rev |
| | 2013 S-Series Shark Bay 14 15 17 | | 1 |
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EMI Caps



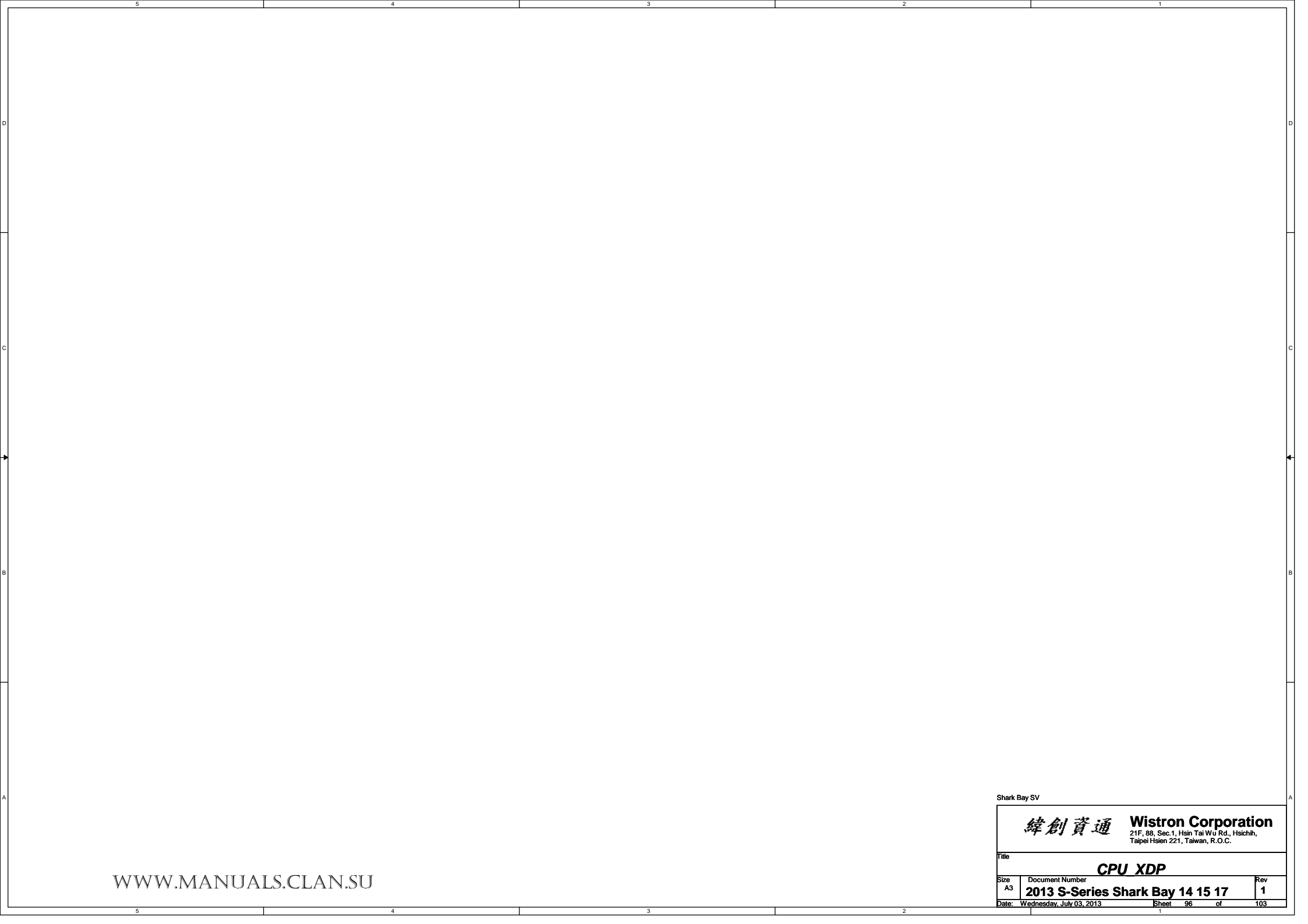


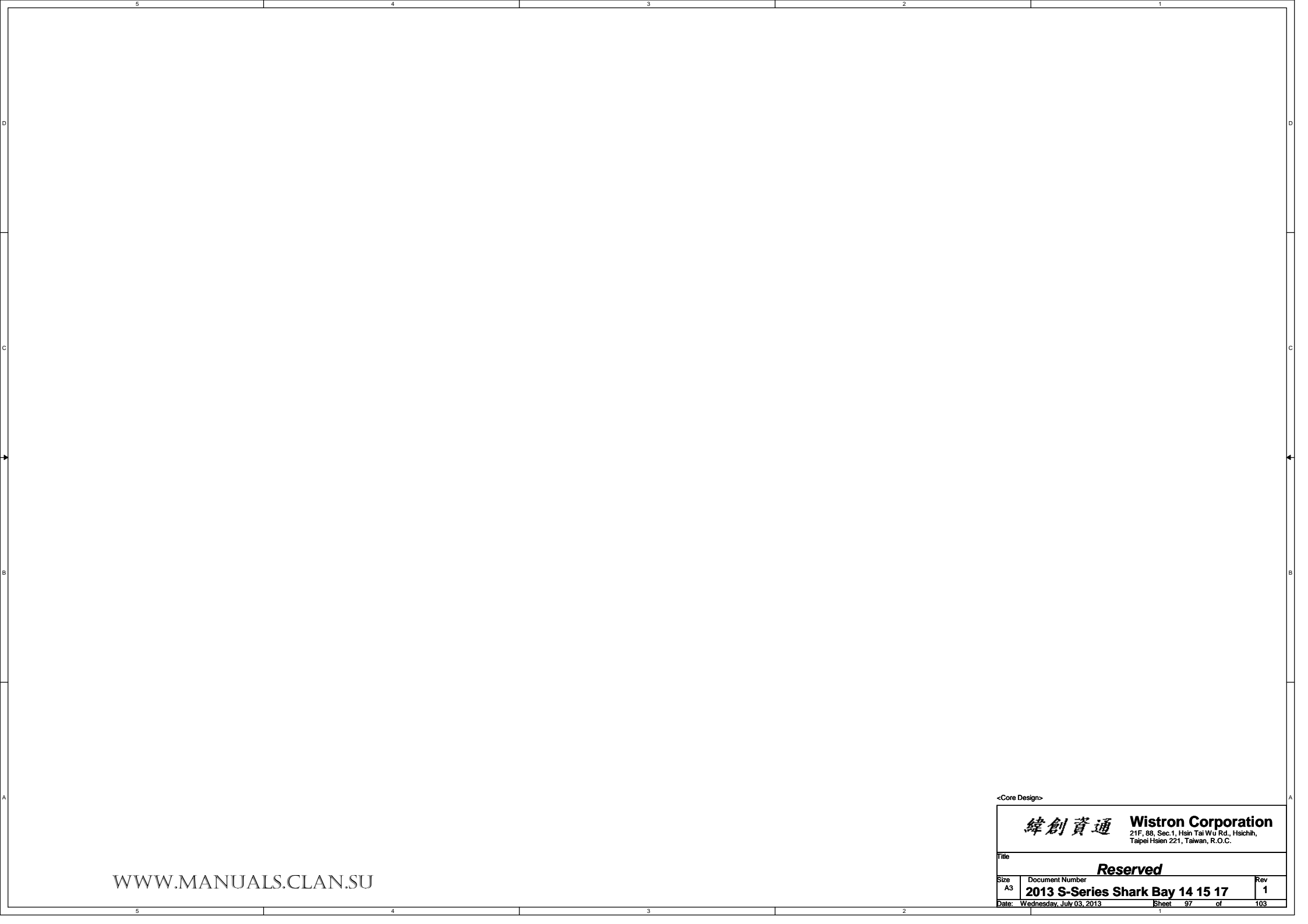
<Variant Name>

| | | | |
|-------------|--------------------------------|---|-------------|
| 緯創資通 | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsuehshih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | | |
| TPM | | | |
| Size | Document Number | Rev | |
| Custom | 2013 S-Series Shark Bay | | 1415 |
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<Core Design>

緯創資通

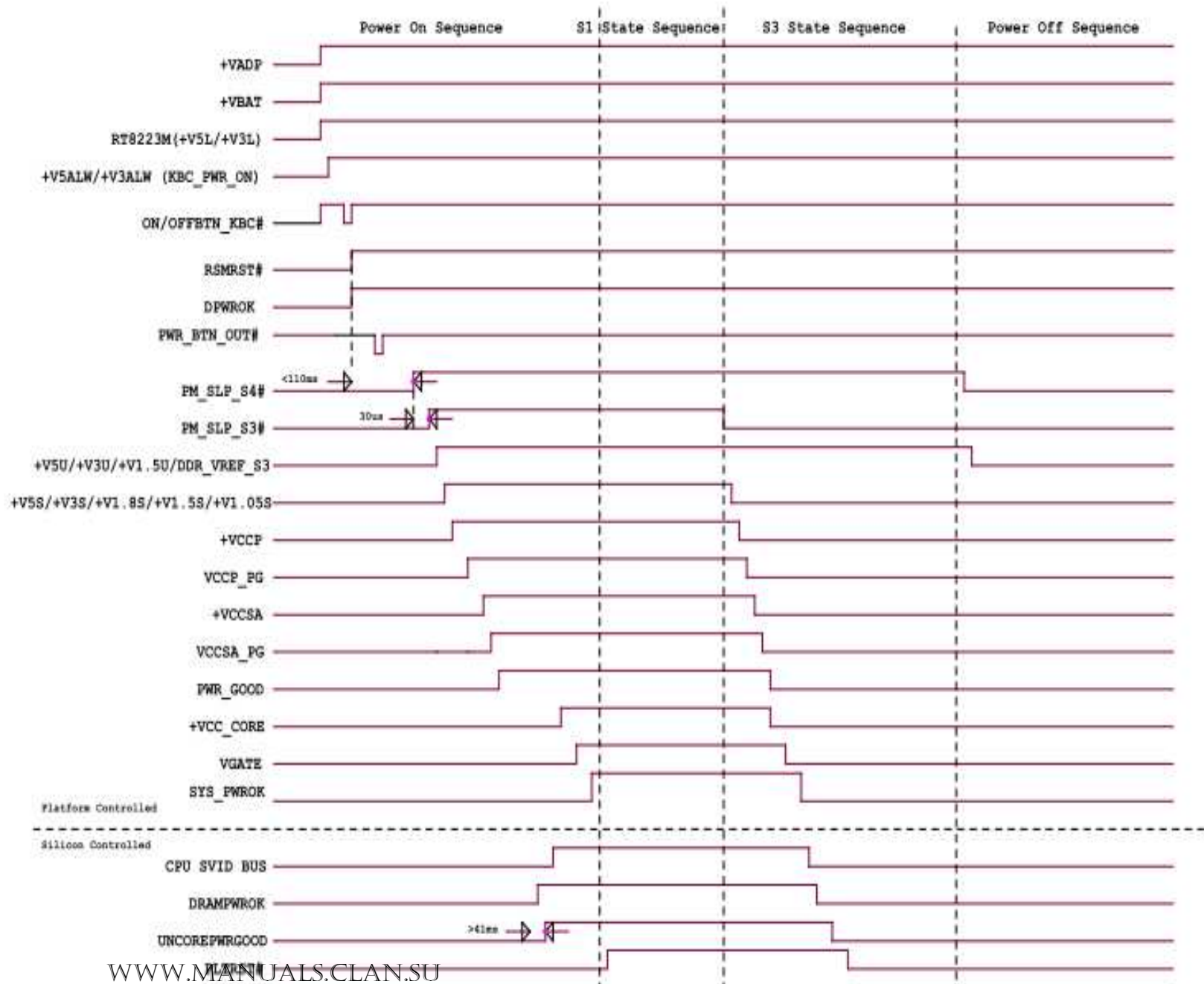
Wistron Corporation
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Title

Change History

| | | |
|-------|--------------------------------|-----------------|
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S-Series Power Sequence and Reset Signal Timing



<Core Design>

緯創資通 Wistron Corporation
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Title

Power Sequence

Size
A3

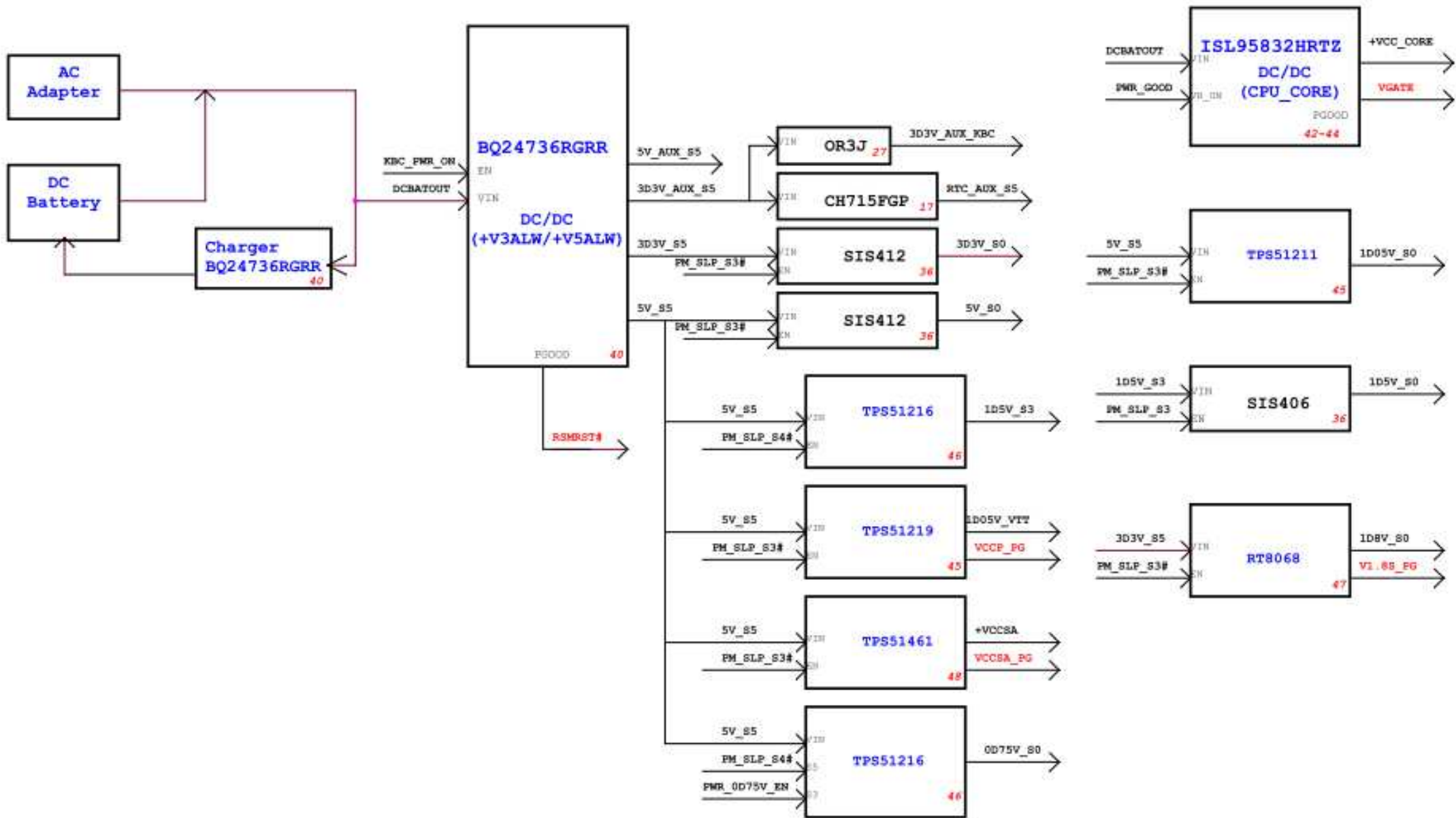
Document Number

2013 S-Series Shark Bay 14115 17

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S-Series POWER BLOCK DIAGRAM



<Core Design>

緯創資通 **Wistron Corporation**
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Title

Power Block Diagram

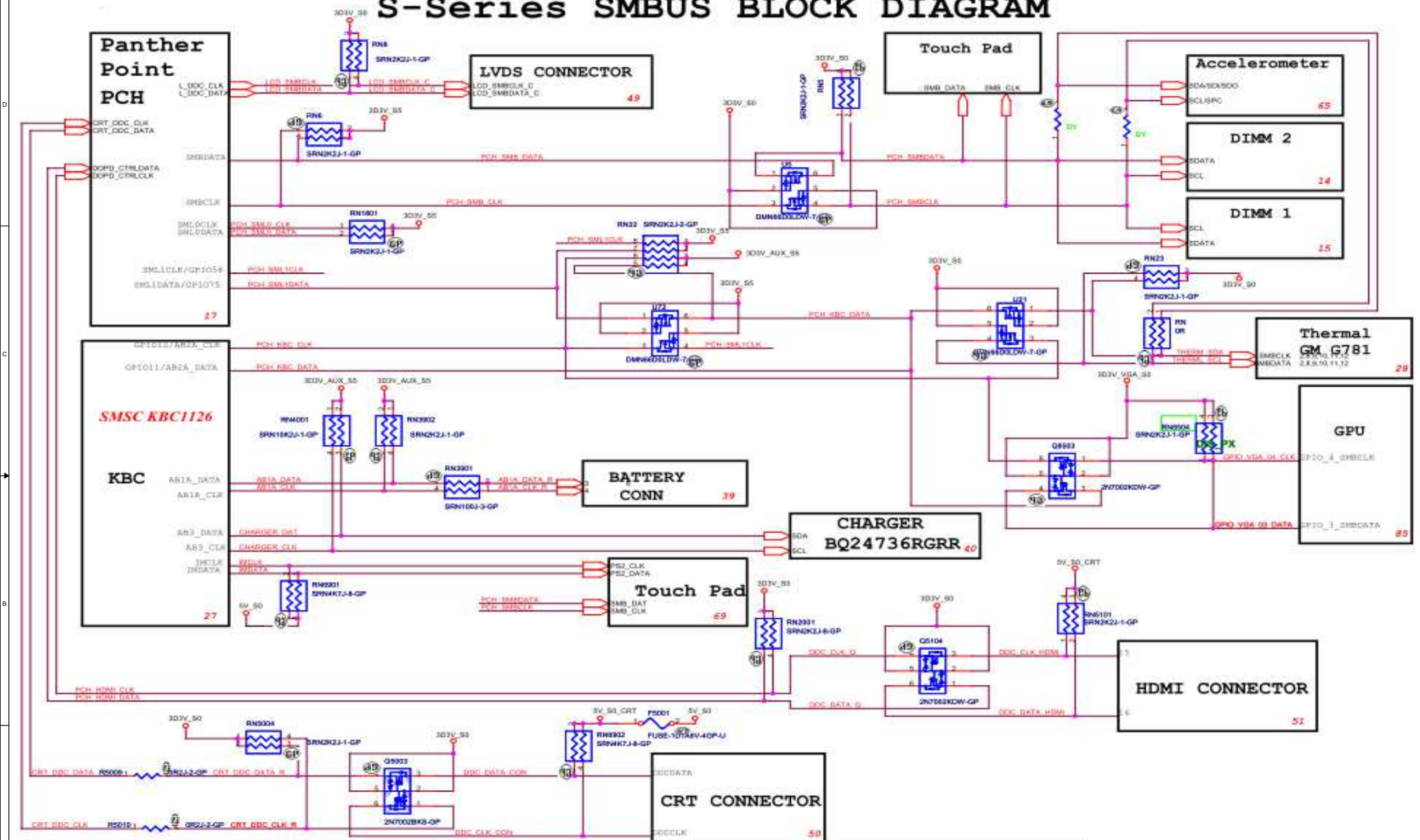
| Size | Document Number |
|------|-----------------|
|------|-----------------|

2013 S-Series Shark Bay 14¹⁵ 17

Date: Wednesday, July 03, 2013

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S-Series SMBUS BLOCK DIAGRAM

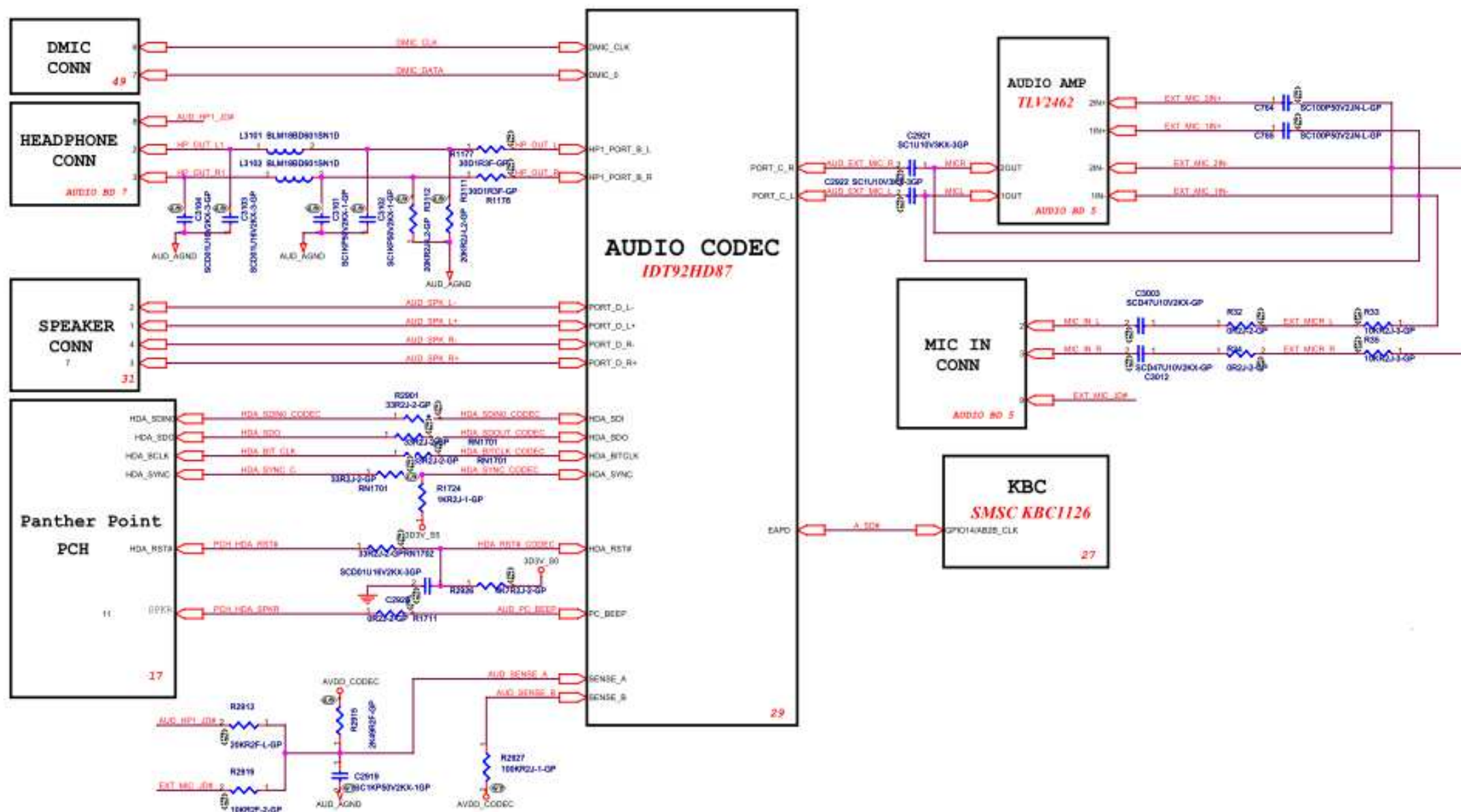


<Core Design>

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| | | | |
|-------|--------------------------|-------|------------|
| File | SMBUS Block Diagram | | |
| Size | Document Number | Rev | |
| A3 | | | |
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S-Series AUDIO BLOCK DIAGRAM



<Core Design>

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| | |
|-------|------------------------------------|
| Title | Thermal/Audio Block Diagram |
|-------|------------------------------------|

| | | |
|-------------------------------|------------------|----------|
| Size A3 | Document Number | Rev |
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Title

Size
A3

Document Number

Rev

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